Photocoupler Synchronous Rectifier Controller IC

Product Description

The EMD2A688 is a synchronous rectifier controller IC which combines an AlGaInP Red emitting diode and smart logic system for controlling secondary side rectifying power MOSFET. The control system can improve efficiency on switching power supply system. The most common application is on fast-charging system.

Applications

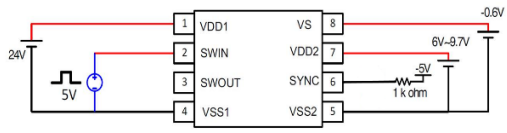
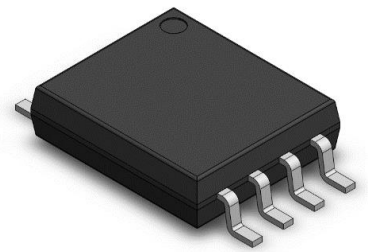
- Switching Power Supply Unit

Features

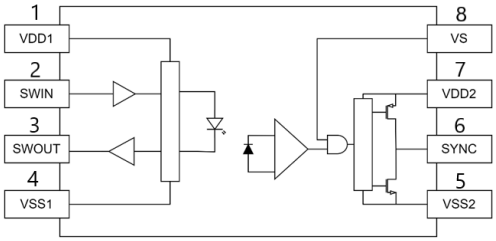
- High isolation 5000V RMS
- Synchronous control on switching power supply system
- Operating temperature range -40°C ~110°C
- REACH & RoHS compliance
- MSL Class 1

Safety approved

- Regulatory Approvals
  - UL - UL1577
    Certificate No. E529603
  - VDE - EN60747-5-5(VDE0884-5)
  - CQC – GB4943.1, 2022
    Certificate No.
    CQC24001437590

SCHEMATIC	PIN DEFINITION	PACKAGE
	1. VDD1 2. SWIN 3. SWOUT 4. VSS1 5. VSS2 6. SYNC 7. VDD2 8. VS	

Connection Diagram



Order Information

EMD2A688(SK08/SL08)-ZV

EMD – Company Abbr.

2A – Stack

688 – Part Number

SK08/SL08 – Lead Form Option

(SK08-9mm Clearance or SL08-11mm Clearance)

Z – Tape and Reel Option (R1/R2)

V – VDE Option (V or None)

Order, Mark & Packing Information

Package	Product ID	Mark		Packing
LSOP-8	EMD2A688SK08-R1V EMD2A688SL08-R1V		E : ESMT YY : Date code (Year) WW : Date code (Week) 688 : Part Number H : Internal Tracking Code V : VDE Option (V or None)	Tape & Reel 3Kpcs
	EMD2A688SK08-R1 EMD2A688SL08-R1			

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Max	Unit
Storage temperature	TSTG	-55	125	°C
Operating temperature	TOPR	-40	110	°C
ISYNC peak output current (1)	ISYNC	0.6		A
Supply Voltage	VDD1 – VSS1	27		V
	VDD2 – VSS2	35		
VSYNC Output voltage	VSYNC	0 to VDD2		V
VS Sensing Voltage	VS	-0.6~+0.6		V
VSWIN input Voltage	VSWIN	-0.5~VDD1		V
VSWOUT output voltage	VSWOUT	0~VDD1		V
ESD, human body mode(2)	VESD_HBM	≥2K (Class 3A)		V
ESD, machine mode(3)	VESD_MM	≥100		V
Latch-up reliability(4)	Latch-Up	Class I		-
Supply over voltage(4)	VSO	VDD1>36 VDD2>42		V

Note 1. Exponential waveform, pulse width < 0.3μs, f=15KHz. This value is intended to allow for component tolerances for designs with IOP minimum 0.6A.
Note 2. MIL-STD-883H Method NO. 3015.8
Note 3. ANSI/ESD S5.2-2009
Note 4. JEDEC STD NO.78/78C

Recommended Operation Condition

Parameter	Symbol	Min	Max	Unit
Ambient operating temperature	T_A	-40	110	°C
Primary side supply voltage	VDD1 -VSS1	12	24	V
Secondary side supply voltage	VDD2 -VSS2	10	30	V
VSWIN Input Voltage	VSWIN	-0.6	24	V
VSWOUT Output Voltage	VSWOUT	0	VDD1	V
VSYNC Output Voltage	VSYNC	0	VDD2	V
SR MOS Source Terminal voltage Sensing	VS	-0.6	0.6	V
ISWOUT Peak high-level output current	| IOPH1 |	-	1.0	A
ISWOUT Peak low-level output current (7)	| IOPL1 |	-	1.0	A
ISYNC Peak high-level output current (7)	| IOPH2 |	-	0.6	A
ISYNC Peak low-level output current (7)	| IOPL2 |	-	0.6	A

Note 5. The rise and fall time of the input current must be less than 50nS.
Note 6. Denote the operating range, not the recommended operating conditions.
Note 7. Exponential waveform with the pulse width of IOP greater than 0.6A being less than 0.3μs and T_A=110°C.

Electrical Characteristics

All Typical values at T_A = 25°C and V_{DD1} = V_{DD2} = 20 V, unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
SYNC High-level output current	IOH			-0.3	A	V_O = V_{DD2} – 2.0V V_O = V_{DD2} – 6.0V
				-0.6		
SWOUT High-level output current				-0.5	A	V_O = V_{DD1} – 2.0V
				-1.0		V_O = V_{DD1} – 6.0V
SYNC Low-level output current	IOL	0.3			A	V_O = V_{SS2} + 2.0V
		0.6				V_O = V_{SS2} + 6.0V
SWOUT Low-level output current		0.5			A	V_O = V_{SS1} + 2.0V
		1.0				V_O = V_{SS1} + 6.0V
SYNC High-level output voltage	VOH	V_{DD2} – 6.0V	V_{DD2} – 3.0V		V	I_O = -0.6A
		V_{DD2} – 0.8V	V_{DD2} - 0.4V			I_O = -100mA
SWOUT High-level output voltage		V_{DD1} – 6.0V	V_{DD1} – 3.0V		V	I_O = -1.0A
		V_{DD1} – 0.6V	V_{DD1} - 0.6V			I_O = -100mA
SYNC Low-level output voltage	VOL		V_{SS2} + 4.0V	V_{SS2} + 6.0V	V	I_O = 0.6A
			V_{SS2} + 0.5V	V_{SS2} + 1.0V		I_O = 100mA
SWOUT Low-level output voltage			V_{SS1} + 4.0V	V_{SS1} + 6.0V	V	I_O = 1.0A
			V_{SS1} + 0.3V	V_{SS1} + 0.5V		I_O = 100mA
VDD1 high-level supply current	IDDH1		0.5	0.8	mA	V_{SWIN}=5.0V
VDD1 low-level supply current	IDDL1		2.0	4.0	mA	V_{SWIN}=0.0V
VDD2 high-level supply current	IDDH2		3.5	5	mA	LED=ON
VDD2 low-level supply current	IDDL2		3.0	5	mA	LED=OFF
VSYNC turn off threshold	V_{THOFF}	10	-5	-25	mV	
VSWIN input high threshold	VIH	2.2	2.76	3.5	V	
VSWIN input low threshold	VIL	2	2.62	3.3	V	
HO, LO Output low peak current HO, LO Output high peak current	VUVLO1+	8.9	9.7	10.5	V	
	VUVLO1-	8.3	9.0	9.8		
VDD1 high-level supply current	UVLOHYS1		0.5		V	
VDD2 under voltage lockout Threshold	VUVLO2+	6.9	7.8	8.8	V	
	VUVLO2–	5.9	6.7	7.6		
VDD2 under voltage lockout threshold hysteresis	UVLOHYS2		1.1		V	

Switching Specification

All Typical values at T_A = 25°C and V_{DD1} = V_{DD2} = 20 V, unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
Propagation delay time VSWIN to VSWOUT output low	t_{PDHL1}	-	130	250	ns	
Propagation delay time VSWIN to VSWOUT output high	t_{PDLH1}		150	250	ns	
Propagation delay time VSWIN to VSYNC output low	t_{PDHL2}	-	85	380	ns	
Propagation delay time VSWIN to VSYNC output high	t_{PDLH2}		100	380	ns	
VSYNC rise time (10% – 90%)	t_f	-	3.5	30	ns	
VSYNC fall time (90% – 10%)	t_r	-	7	30	ns	
VSYNC turn off propagation, from VTHOFF	t_{DOFF}		50	100	ns	
SR MOS ON-Blanking Time	Tblanking		500	1000	ns	
SWIN rising detection	Tdetect		500	800	ns	
VDD1 UVLO turn-on delay	t_{UVLO1} ON	-	3.8	-	µs	ICC1 > 1mA
VDD1 UVLO turn-off delay	t_{UVLO1} OFF	-	3	-	µs	ICC1 < 1mA
VDD2 UVLO turn-on delay	t_{UVLO2} ON	-	4	-	µs	LED=ON , V_{SYNC} > 5V
VDD2 UVLO turn-off delay	t_{UVLO2} OFF	-	4	-	µs	LED=ON , V_{SYNC} < 5V
Logic High Common Mode Transient Immunity	|CMH|	10	-	-	kV/µs	|VCM| = 1.5kV , LED=ON, VDD2 = 20 V, T_A = 25° C
Logic Low Common Mode Transient Immunity	|CML|	10	-	-	kV/µs	|VCM| = 1.5kV, LED=OFF, VDD2 = 20 V, T_A = 25° C

Isolation characteristic

All Typical values at T_A = 25°C and V_{DD2}= 20 V, unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Condition
Withstand Insulation Test Voltage (Note 8, 9)	V_{ISO}	EMD2A688-SK EMD2A688-SL	5000	-	-	V	RH ≤ 40%-60%, t = 1min, T_A = 25 °C
Input-Output Resistance (Note 9)	R_{I-O}	-	-	10^{12}	-	Ω	V_{I-O} = 500V DC

Note 8: Device is considered a two terminal device: pins 1, 2, 3, 4 are shorted together and pins 5, 6, 7, 8 are shorted together.

Note 9: According to UL1577, each photo coupler is tested by applying an insulation test voltage 6000VRMS for one second. This test is performed before the 100% production test for partial discharge.

Typical Performance Curves & Test Circuits

Fig.1 High output rail voltage vs. Temperature

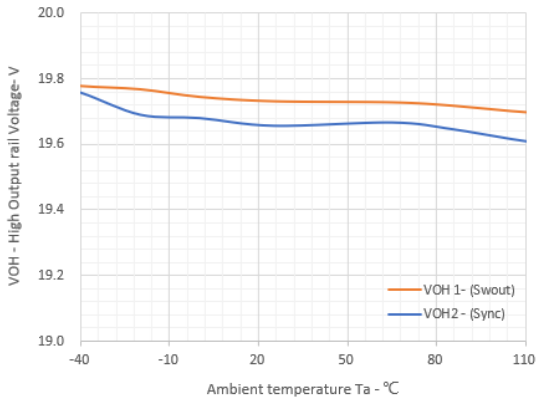


Fig.2 IDD vs. Temperature

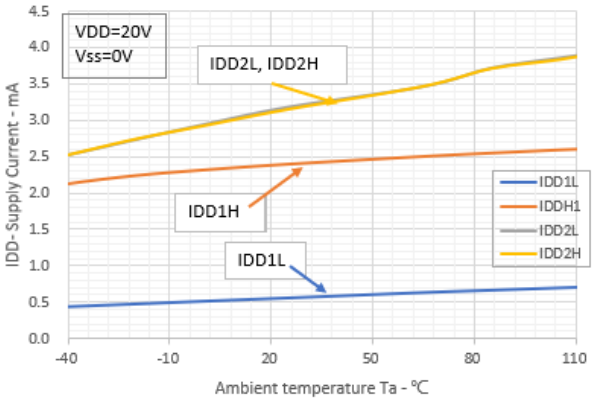


Fig.3 IDD vs. VDD

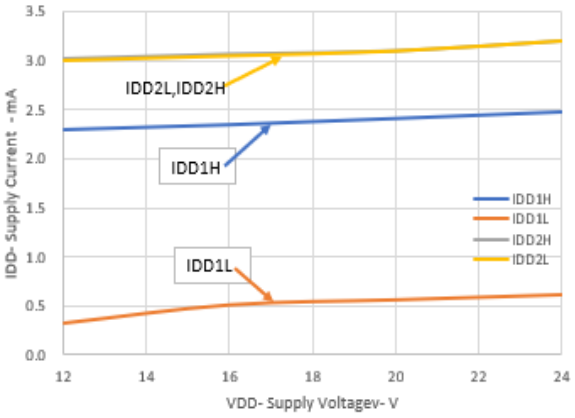


Fig.4 VinLH vs. Hysteresis

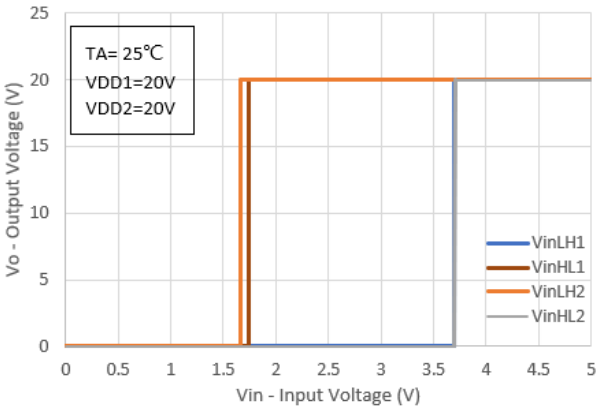


Fig.5. VinLH vs. Temperature

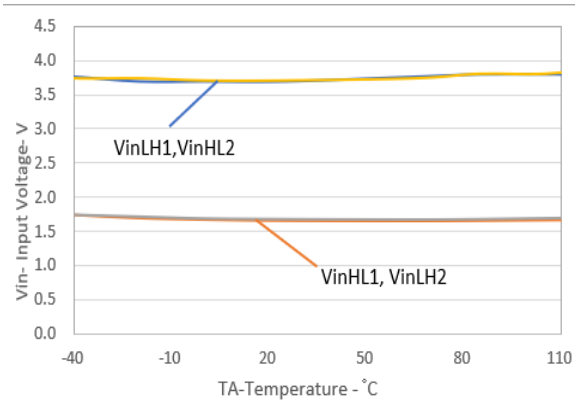


Fig.6 Propagation Delays vs. Vcc

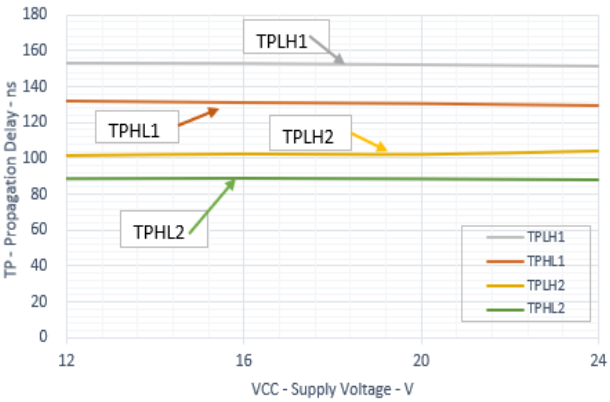
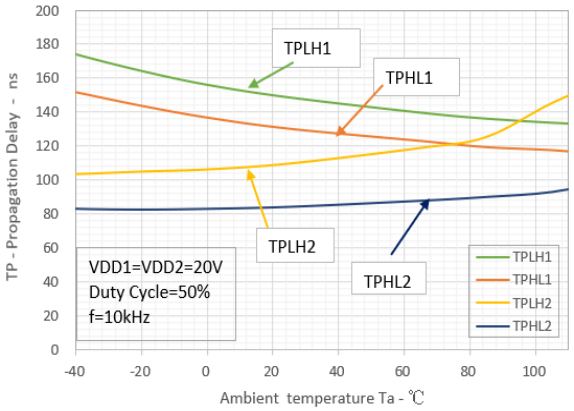
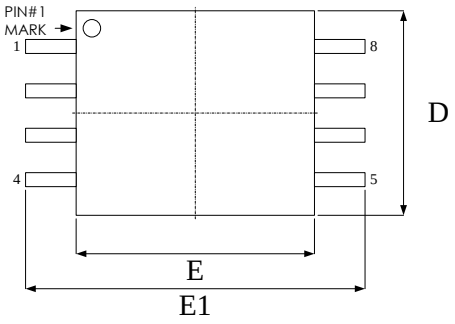


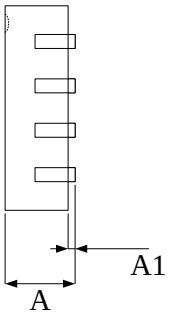
Fig.7 Propagation Delay vs. Temperature	
	

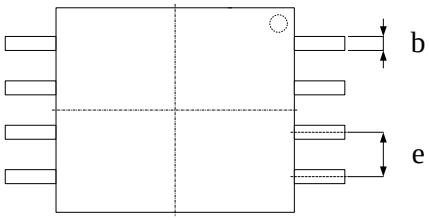
Package Outline Drawing

L-SOP 8LDS (277mil, 9mm clearance)(SK08)

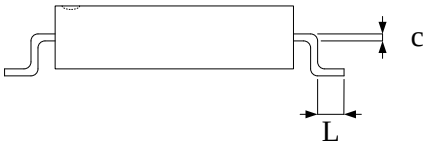


TOP VIEW





BOTTOM VIEW

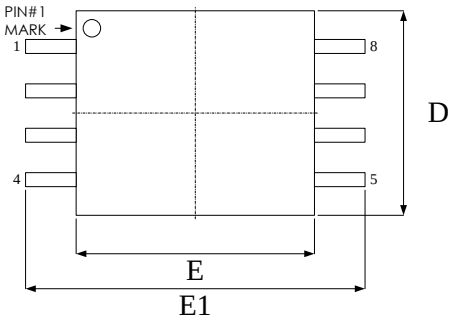


SIDE VIEW

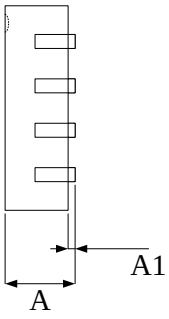
Symbol	Dimension in mm	
	Min.	Max.
A	1.70	2.30
A1	0.10	0.30
b	0.30	0.50
c	0.10	0.30
D	5.55	6.15
E	6.51	7.11
E1	9.30	10.10
e	1.27 BSC	
L	0.75	-

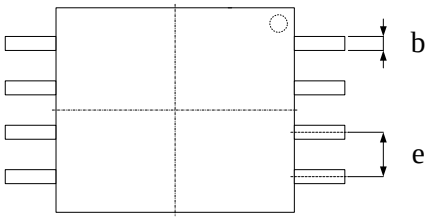
Package Outline Drawing

L-SOP 8LDS (277mil, 11mm clearance)(SL08)

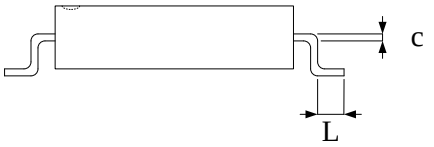


TOP VIEW





BOTTOM VIEW



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b	0.30	0.50
c	0.10	0.30
D	5.55	6.15
E	6.51	7.11
E1	11.20	11.80
e	1.27 BSC	
L	0.75	-

Revision History

Revision	Date	Description
1.0	2025.04.22	Original.
1.1	2025.10.07	Update purchase order number's suffix
1.2	2025.10.30	Update Connection Diagram/ Schematics

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