

## 2-Vrms Cap-Less Line Driver with Adjustable Gain

### Features

- Operation Voltage: 3.0V to 3.6V
- Cap-less Output
  - Eliminates Output Capacitors
  - Improves Low Frequency Response
  - Reduces POP/Clicks
  - Reduce Board Area and Component Cost
- Low Noise and THD
  - Typical SNR 107dB
  - Typical  $V_n$  7 $\mu$ Vrms
  - Typical THD+N < 0.02%
- Maximum Output Voltage Swing into 10k $\Omega$  Load
  - 2Vrms at 3.3V Supply Voltage
- 16 $\Omega$  Output Load Compliant
- Differential Input, single-Ended Output
- External Gain Setting from 1V/V to 10V/V
- Fast Start-up Time : 0.5ms
- Integrated De-Pop Control
- External Under Voltage Protection
- Thermal Protection
- Active Mute Control for Pop-less Audio ON/OFF Control
- +/-8kV IEC ESD Protection at line outputs

### Applications

- LCD / PDP TVs
- CD / DVD players
- Set-Top Boxes
- Home Theater in Box

### Description

The AD22653B is a 2-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

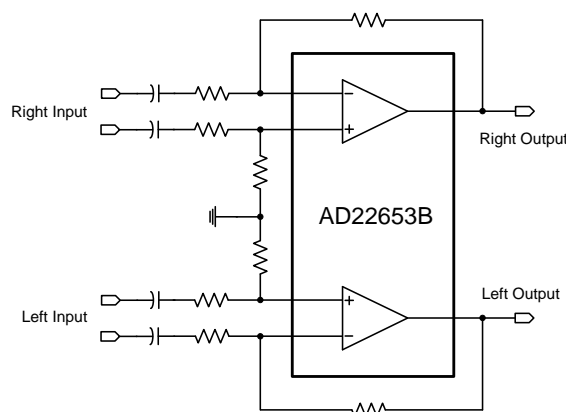
The AD22653B is capable of delivering 2-Vrms output into a 10k $\Omega$  load with 3.3V supply. The gain settings can be set by users from  $\pm 1V/V$  to  $\pm 10V/V$  externally, and gain can be configured individually for R/L channel. The AD22653B has built-in active-mute control for pop-less audio on/off control. The AD22653B has internal and external under voltage protection to prevent POP noise. Built-in de-pop control sequence also help AD22653B to be a pop-less device.

The AD22653B is available in a 14-pin TSSOP package.

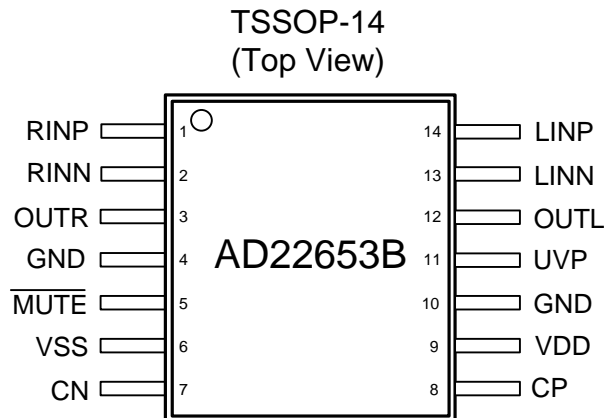
### Ordering Information

Product ID	Package	Packing	Comments
AD22653B-QH14NAT	TSSOP-14	96 Units / Tube	Green (HF)
AD22653B-QH14NAR		100 Tubes / Small Box	
		2.5k Units Tape & Reel	

### Simplified Application Circuit



## Pin Assignments

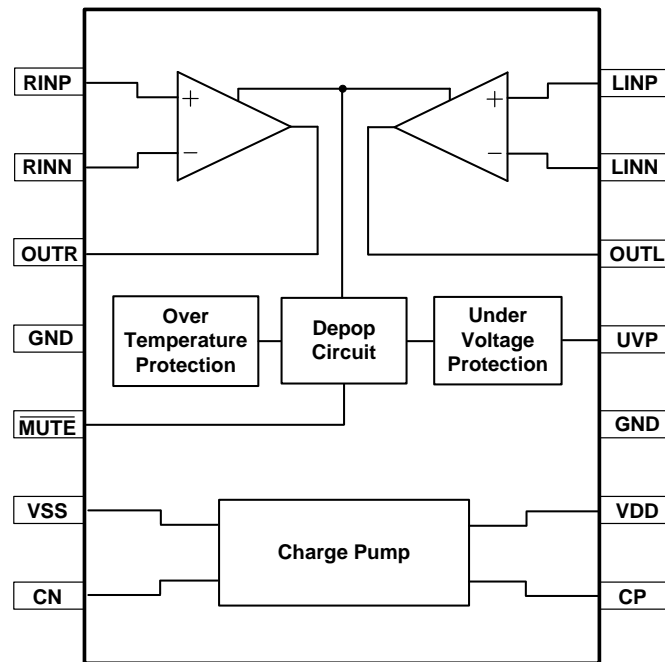


## Pin Description

No.	Name	Type <sup>(1)</sup>	Pin Description
1	RINP	I	Right channel OP positive input
2	RINN	I	Right channel OP negative input
3	OUTR	O	Right channel OP output
4	SGND	P	Signal ground
5	$\overline{\text{MUTE}}$	I	Mute, active low
6	PVSS	P	Supply voltage
7	CN	I/O	Charge-pump flying capacitor negative terminal
8	CP	I/O	Charge-pump flying capacitor positive terminal
9	PVDD	P	Positive supply
10	PGND	P	Power ground
11	UVP	I	Under-voltage protection input, internally pulled high
12	OUTL	O	Left channel OP output
13	LINN	I	Left channel OP negative input
14	LINP	I	Left channel OP positive input

(1) I=input, O=output, P=power

## Functional Block Diagram



## Available Package

Package Type	Device No.	$\Theta_{ja}$ (°C/W) <sup>(1)</sup>	$\Theta_{jc}$ (°C/W) <sup>(2)</sup>
TSSOP-14	AD22653B	100	32

(1)  $\Theta_{ja}$  is measured at room temperature ( $T_A=25^\circ\text{C}$ ), natural convection environment test board, which is constructed with a thermal efficient, 2-layers PCB. The measurement is tested using the JEDEC51-3 thermal measurement standard.

(2)  $\Theta_{jc}$  represents the heat resistance for the heat flow between the chip and package's top surface.

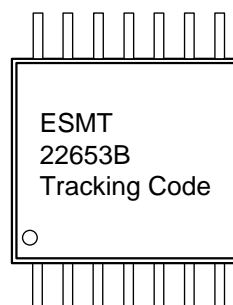
## Marking Information

AD22653B

Line 1 : LOGO

Line 2 : Product No.

Line 3 : Tracking Code



## Absolute Maximum Ratings<sup>(1)</sup>

SYMBOL	PARAMETER	VALUE	UNIT
	Supply Voltage, $V_{DD}$ to GND	-0.3 to 3.6	V
$V_I$	Input Voltage	VSS -0.3 to VDD+0.3	V
$R_L$	Minimum load impedance	16	$\Omega$
	$\overline{MUTE}$ to GND	-0.3 to VDD+0.3	V
$T_{stg}$	Storage temperature range	-65 to 150	$^{\circ}\text{C}$
$T_J$	Maximum operating junction temperature range	-40 to 150	$^{\circ}\text{C}$

(1) The absolute maximum ratings are limiting values of operation, safety of the device cannot be guaranteed if beyond those values.

## Recommended Operating Conditions

SYMBOL	PARAMETER	Min	NOM	Max	UNIT
$V_{DD}$	Supply Voltage	3.0	3.3	3.6	V
$V_{IH}$	High Level Input Voltage		60		% of $V_{DD}$
$V_{IL}$	Low Level Input Voltage		40		% of $V_{DD}$
$T_A$	Operating Ambient Temperature Range	-40		85	$^{\circ}\text{C}$
$R_L$	Load Resistance	16			$\Omega$

## Electrical Characteristics

PVDD=3.3V,  $T_A=25^{\circ}\text{C}$ ,  $R_L=10\text{k}\Omega$ ,  $C_{FLY}=C_{PVSS}=1\mu\text{F}$ ,  $C_{IN}=1\mu\text{F}$ ,  $R_I=10\text{k}\Omega$ ,  $R_F=20\text{k}\Omega$  (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	Min	NOM	Max	UNIT
$I_{DD}$	$V_{DD}$ Supply Current	$\overline{MUTE}=V_{DD}$		7	15	mA
$I_{SD}$	$V_{DD}$ Shutdown Current	$\overline{MUTE}=0\text{V}$			5	$\mu\text{A}$
$I_I$	Input Current	$\overline{MUTE}$ pin		0.1		$\mu\text{A}$
$V_O$	Output Voltage (Outputs In Phase)	THD+N=1%, $V_{DD}=3.3\text{V}$ , $f_{IN}=1\text{kHz}$	2.0	2.3		Vrms
THD+N	Total Harmonic Distortion Plus Noise	$V_O=2\text{Vrms}$ , $f_{IN}=1\text{kHz}$		0.004		%
Crosstalk	Channel Separation	$V_O=2\text{Vrms}$ , $f_{IN}=1\text{kHz}$		-105		dB
$V_N$	Output Noise	$R_I=10\text{k}$ , $R_F=10\text{k}$		7	15	$\mu\text{Vrms}$
$V_{SR}$	Slew Rate			8		V/ $\mu\text{s}$
SNR	Signal to Noise Ratio	$V_O=2\text{Vrms}$ , $R_I=10\text{k}$ , $R_F=10\text{k}$ , A-weighted	90	107		dB
$G_{BW}$	Unit-Gain Bandwidth			8		MHz
$A_{VO}$	Open-Loop Gain		80			dB
$V_{OS}$	Output Offset Voltage	$V_{DD}=3.0\text{V to }3.6\text{V}$ , Input Grounded	-1		1	mV

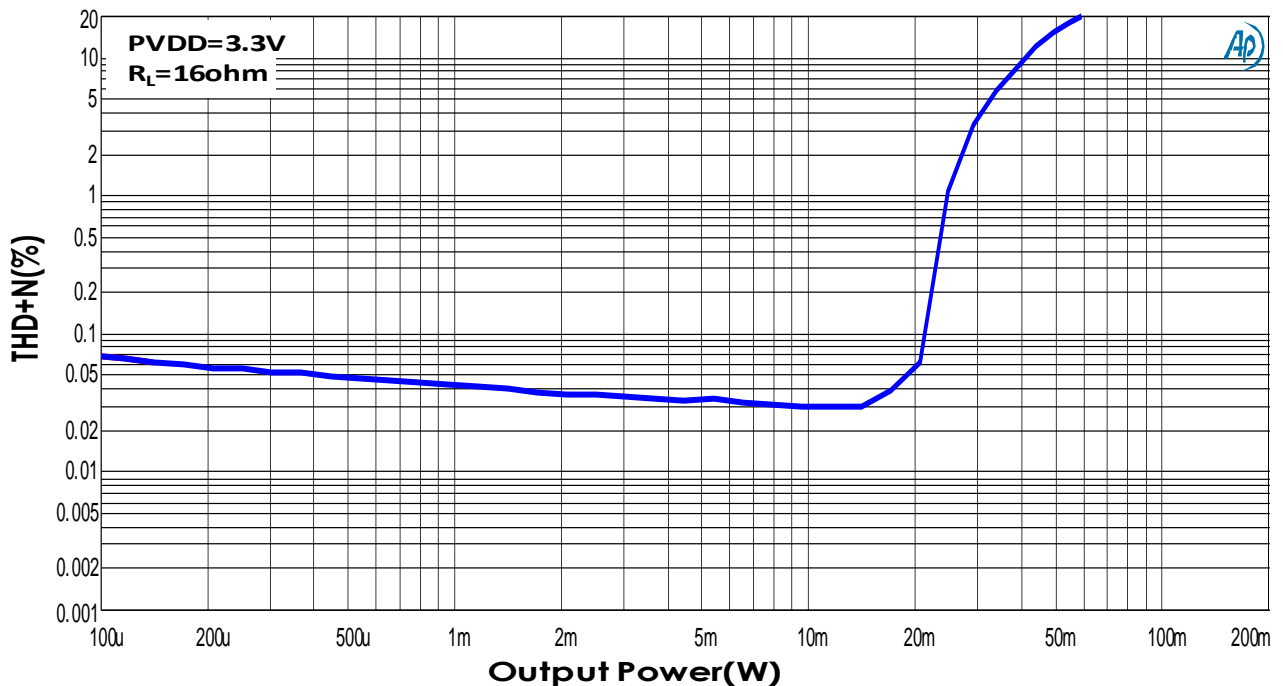
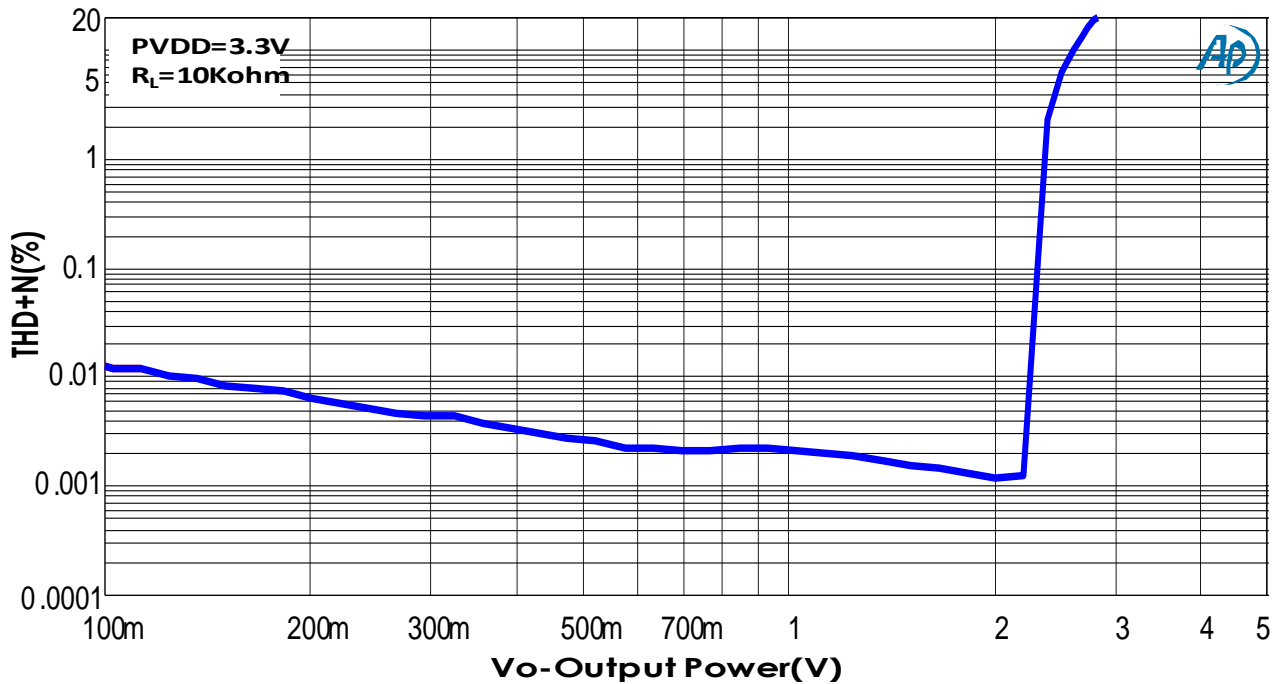
**Electrical Characteristics (Con't)**PVDD=3.3V, T<sub>A</sub>=25°C, R<sub>L</sub>=10kΩ, C<sub>FLY</sub>=C<sub>PVSS</sub>=1μF, C<sub>IN</sub>=1μF, R<sub>I</sub>=10kΩ, R<sub>F</sub>=20kΩ (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	Min	NOM	Max	UNIT
PSRR	Power Supply Rejection Ratio	V <sub>DD</sub> =3.0V to 3.6V, V <sub>rr</sub> =200mVrms, f <sub>IN</sub> =1kHz		-76	-60	dB
R <sub>I</sub>	Input Resistor Range		1	10	47	kΩ
R <sub>F</sub>	Feedback Resistor Range		4.7	20	100	kΩ
f <sub>CP</sub>	Charge-Pump Frequency		400	500	600	kHz
	Maximum capacitive Load			220		pF
V <sub>UVP</sub>	External Under Voltage Detection			1.25		V
I <sub>HYS</sub>	External Under Voltage Detection Hysteresis Current			5		μA
TSD	Over Temperature Protection Level			150		°C
T <sub>start-up</sub>	Start-up Time			0.5		ms

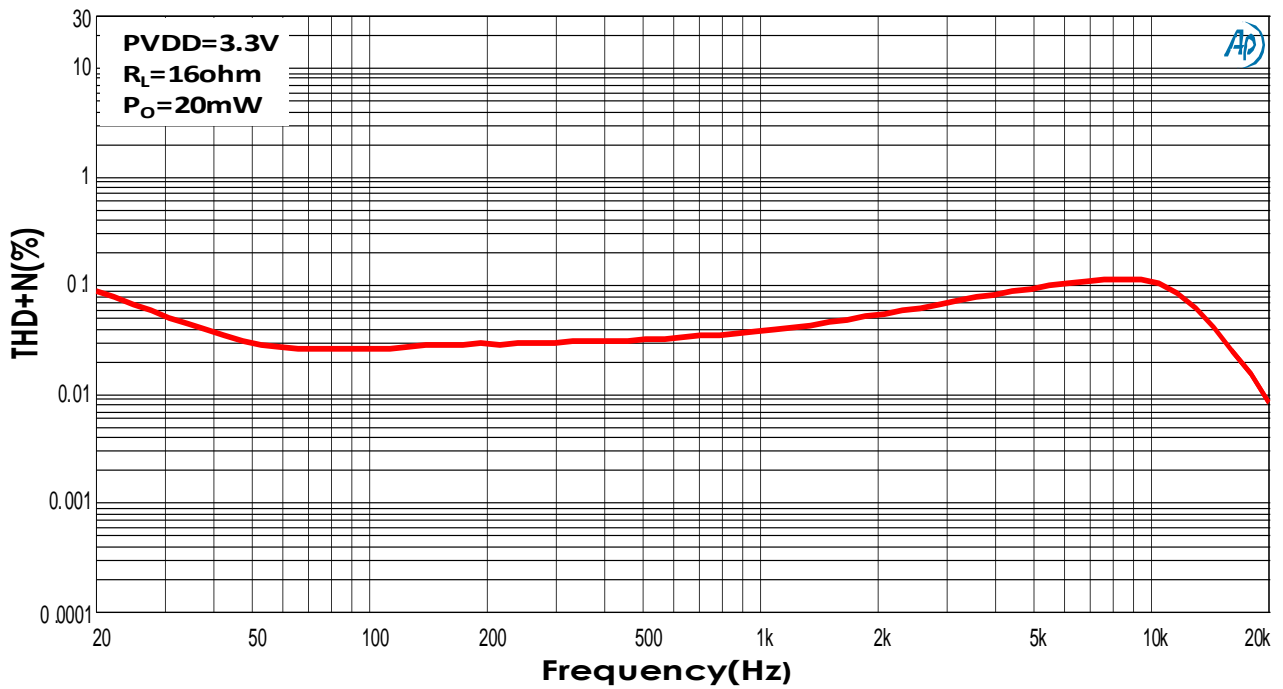
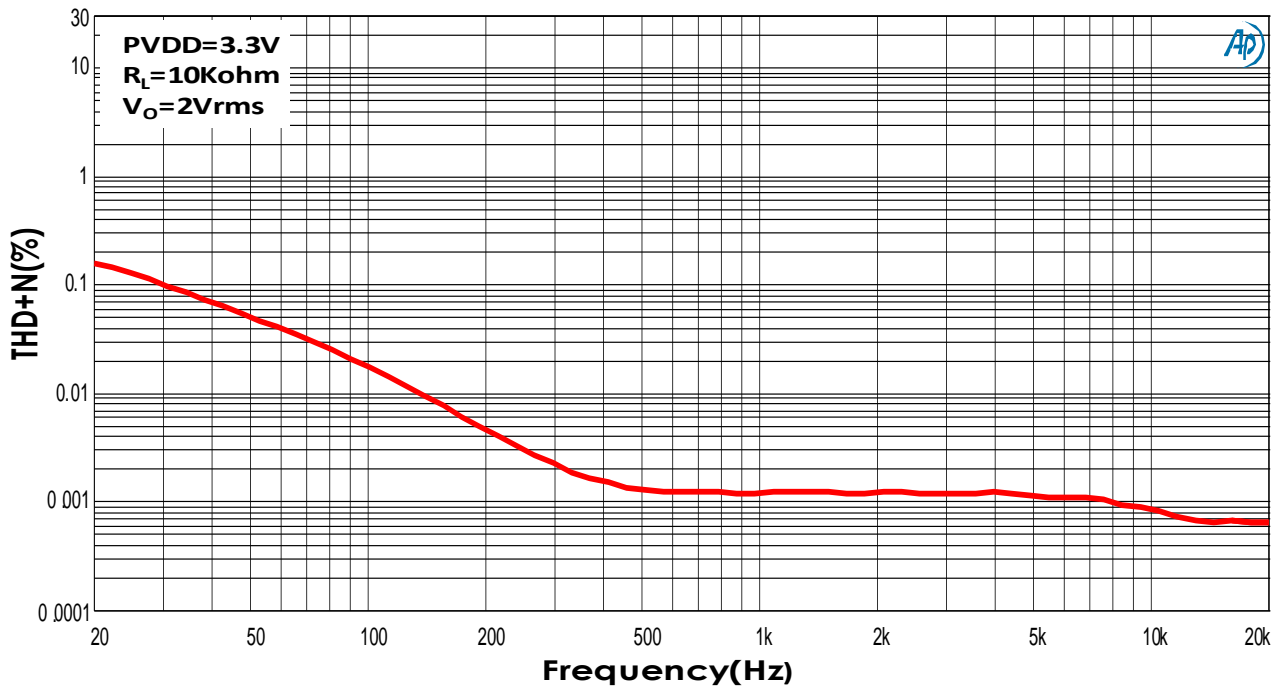
## Typical Characteristics

PVDD=3.3V, T<sub>A</sub>=25°C, R<sub>L</sub>=10kΩ, C<sub>FLY</sub>=C<sub>PVSS</sub>=1μF, C<sub>IN</sub>=1μF, R<sub>I</sub>=10kΩ, R<sub>F</sub>=20kΩ (unless otherwise noted)

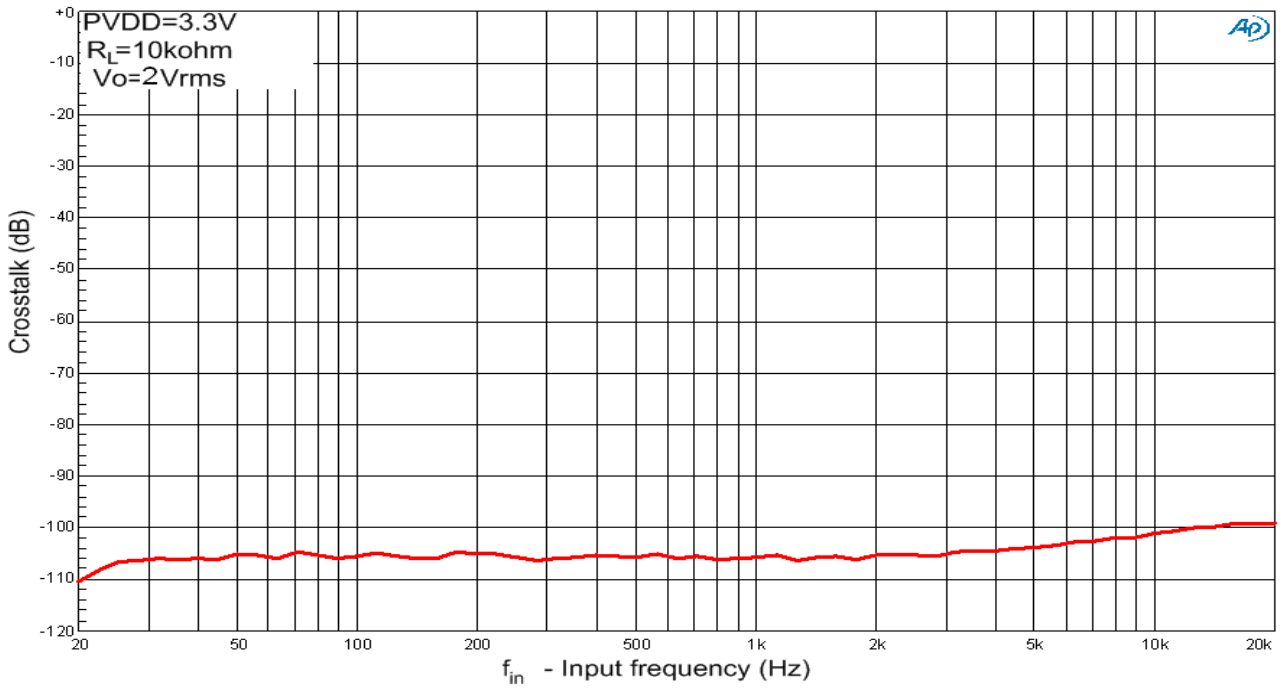
- Total Harmonic Distortion + Noise (THD+N) vs. Output Power



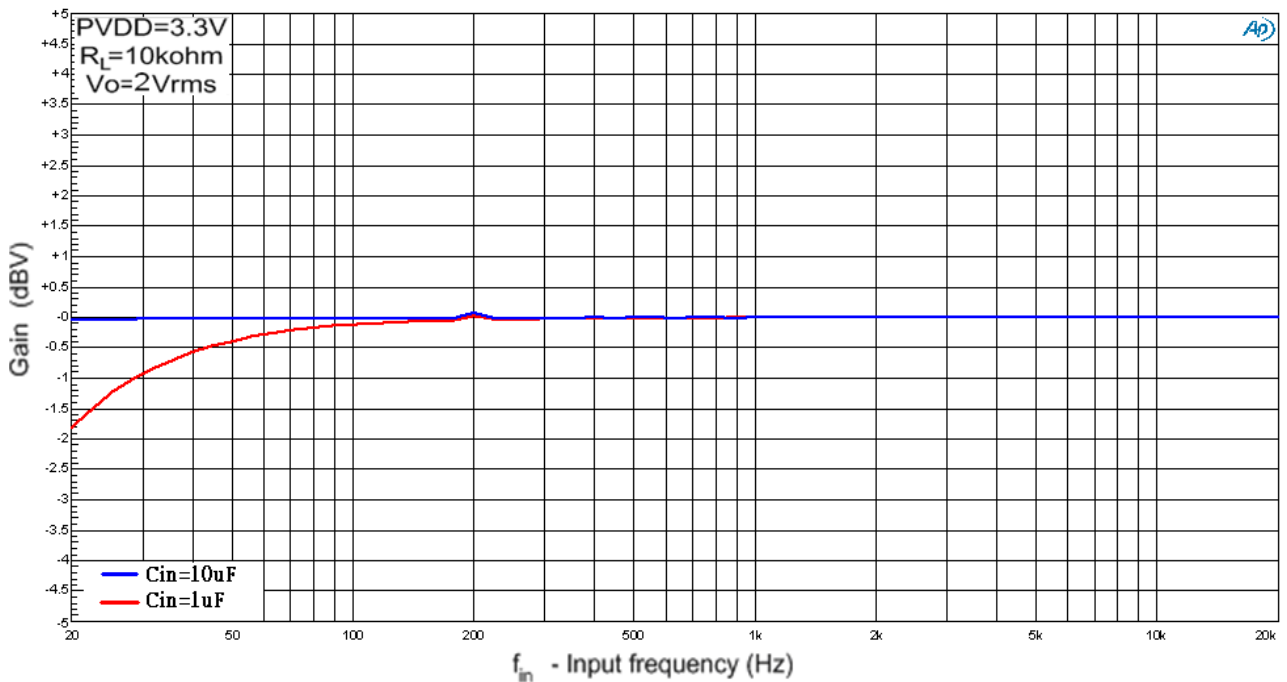
● Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency



## ● Crosstalk vs. Signal Frequency



## ● Gain vs. Signal Frequency





**Application Information**

■ **Line Driver Amplifiers Operation**

A conventional inverting line-driver amplifier always requires an output dc-blocking capacitor and a bypass capacitor, see Figure 1. DC blocking capacitors are large in size and cost a lot. It also restricts the output low frequency response. POP will occur if the charge and discharge processes on output capacitors are not carefully take cared. Besides, it needs to wait for a long time to charge  $V_{OUT}$  from 0V to  $V_{DD}/2$ .

For a cap-less line driver, see figure 2, a negative supply voltage (-VDD) is produced by the integrated charge-pump, and feeds to line driver’s negative supply instead of ground. The positive input can directly connect to ground without a  $C_{BYPASS}$ , and  $V_{OUT}$  is biased at ground which can eliminate the output dc-blocking capacitors. The output voltage swing is doubled compared to conventional amplifiers.

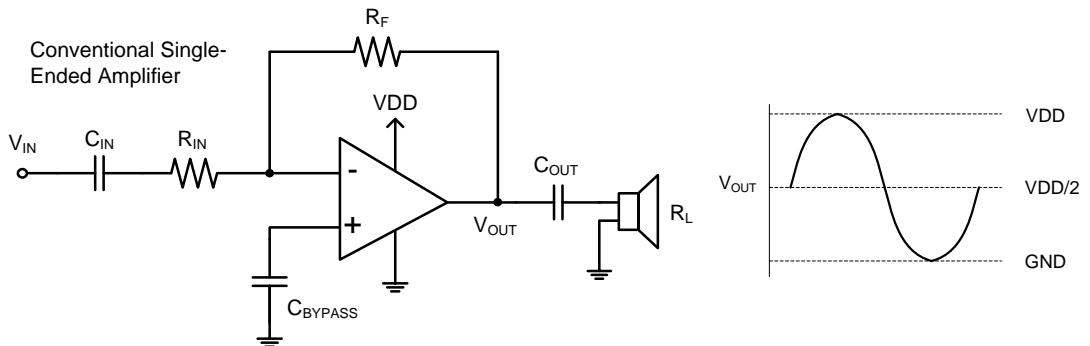


Figure 1. Conventional Line Driver Amplifier

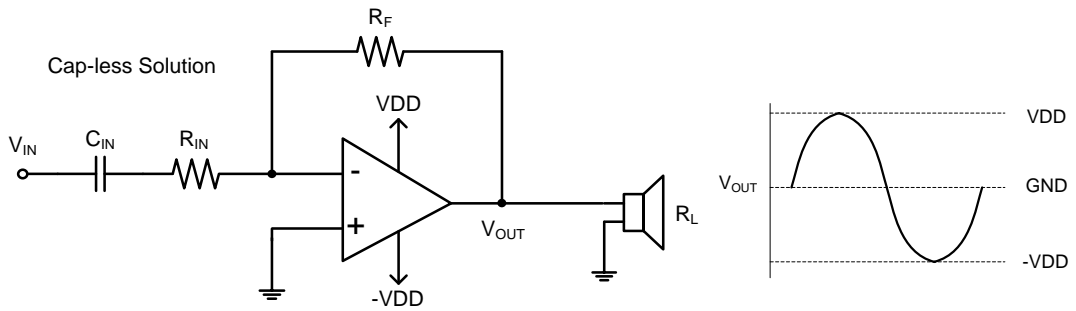


Figure 2. Cap-less Line Driver Amplifier

■ **External Under-Voltage Protection**

The external under-voltage protection is used to mute the line-driver before any input voltage change to generate a POP. The threshold of UVP pin is designed to 1.25V. By using a resistor divider, users can decide the UVP level and hysteresis level. The levels can be obtained by following equations:

$$V_{UVP} = (1.25V - 6\mu A \times R13) \times (R11 + R12) / R12$$

$$Hysteresis = 5\mu A \times R13 \times (R11 + R12) / R12$$

With the condition  $R13 \gg (R11 \parallel R12)$ .

For example, to obtain  $V_{UVP}=2.67V$ ,  $Hysteresis=0.37V$ ,  $R11=1.5k\Omega$ ,  $R12=1k\Omega$ ,  $R13=30k\Omega$ .

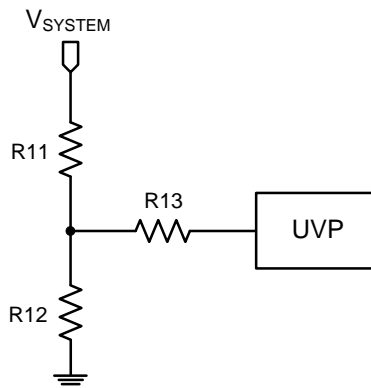
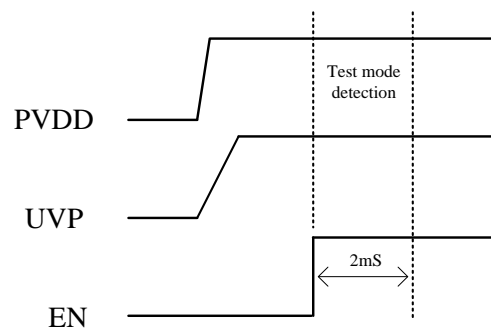
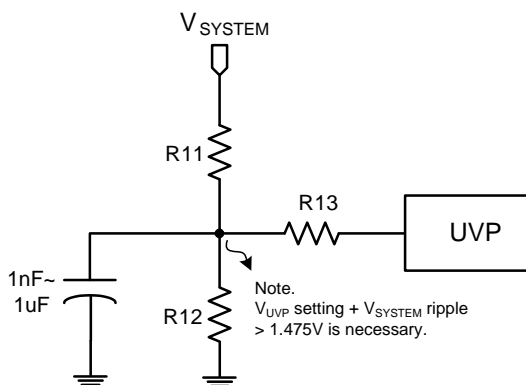


Figure 3-1. Application Circuit of UVP Pin

The UVP pin voltage ripple needs to take care during chip enable state within 2mS. The UVP pin ripple lower 1.25V~1.475V by 2~4 times will trigger test mode in Line Driver. To put a capacitor parallel with UVP pin can improve test mode mis-operating triggered while  $V_{SYSTEM}$  is not stable during power up initially.  $V_{UVP}$  pin voltage threshold  $< 1.475V$  shall be prohibited during chip enable state.



Power on sequence for Line Driver

UVP pin is pulled high internally, and therefore it can be floated to disable the external under-voltage protection feature.

■ **Charge-Pump Operation**

The charge-pump is used to generate a negative supply voltage to supply to line-driver. It needs two external capacitors,  $C_{FLY}$  and  $C_{PVSS}$ , for normal operation, see figure 4 (a). The operation can be analyzed with two phase. In phase I, see figure 4 (b),  $C_{FLY}$  is charged to PVDD, and in phase II, see figure 4 (c), the charges on  $C_{FLY}$  are shared with  $C_{PVSS}$ , that makes PVSS a negative voltage. After an adequate clock cycles, PVSS will be equaled to  $-PVDD$ . Low ESR capacitors are recommended, and the typical value of  $C_{FLY}$  and  $C_{PVSS}$  is  $1\mu F$ . A smaller capacitance can be used, but the maximum output voltage may be reduced.

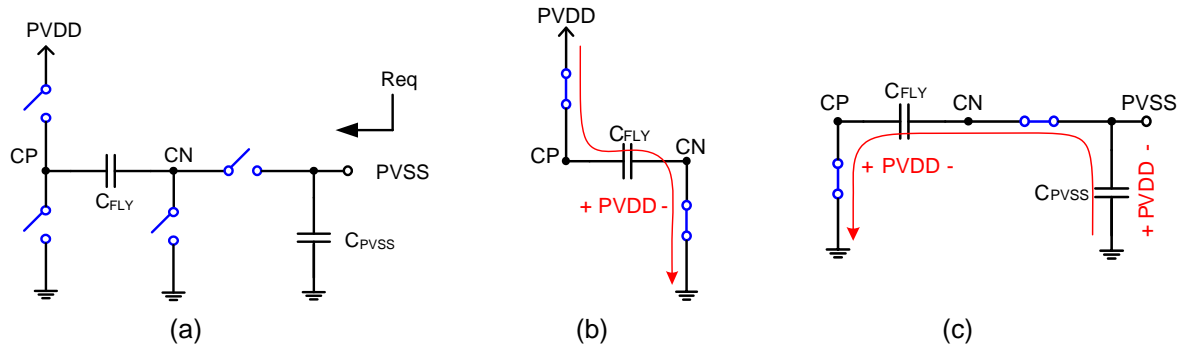


Figure 4. Charge-Pump Operation

■ **Mute Function**

The mute function is used to reduce power consumption while the device is not in use. When a logic low is applied to this pin, the output driver circuits are turned off. Line driver output and PVSS are pulled to ground. When a logic high is applied to mute pin, the PVSS is started to build-up and line driver output signal is released after about 0.5ms typically.

■ **Decoupling Capacitors**

A low ESR power supply decoupling capacitor is required for better performance. The capacitor should place as close to chip as possible, the value is typically  $1\mu F$ . For filtering low frequency noise signals, a  $10\mu F$  or greater capacitor placed near the chip is recommended.

■ **Input Blocking Capacitors ( $C_{IN}$ )**

An input blocking capacitor is required to block the dc voltage of the audio source and allows the input to bias at a proper dc level for optimum operation. The input capacitor and input resistor ( $R_i$ ) form a high-pass filter with the corner frequency determined as following equation:

$$f_c = \frac{1}{2\pi R_i C_{IN}}$$

■ **Gain Setting Resistors ( $R_I$  and  $R_F$ )**

The line driver’s gain is determined by  $R_I$  and  $R_F$ . The typical configurations of the amplifier are inverting, non-inverting, and differential input, see figure 5. The gain equations are listed as follows:

(a) Inverting configuration :  $A_V = -\frac{R_F}{R_I}$

(b) Non-inverting configuration :  $A_V = 1 + \frac{R_F}{R_I}$

(c) Differential-input configuration :  $A_V = \frac{R_F}{R_I}$

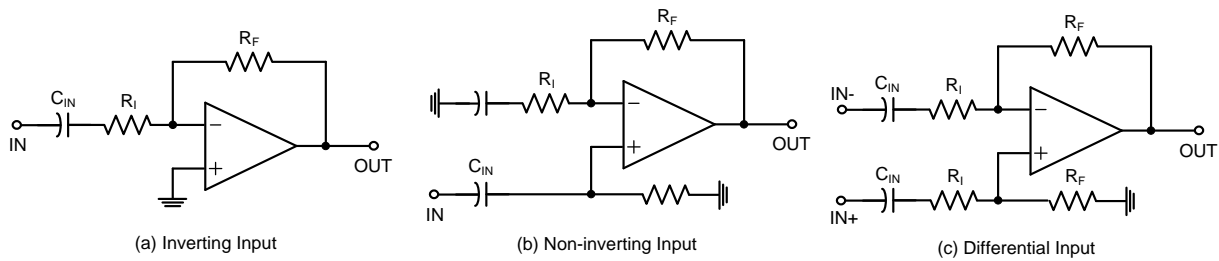


Figure 5. Line Driver Amplifier Configurations

The values of  $R_I$  and  $R_F$  must be chosen with consideration of stability, frequency response and noise. The recommended value of  $R_I$  is in the range from 1k $\Omega$  to 47k $\Omega$ , and  $R_F$  is from 4.7k $\Omega$  to 100k $\Omega$  for. The gain is in the range from -1V/V to -10V/V for inverting configuration. Table 1 lists the recommended resistor values for different configurations.

$R_I$ (k $\Omega$ )	$R_F$ (k $\Omega$ )	Inverting Input Gain (V/V)	Non-inverting Input Gain (V/V)	Differential Input Gain (V/V)
22	22	-1	2	1
15	30	-2	3	2
33	68	-2.1	3.1	2.1
10	100	-10	11	10

Table 1. Recommended Resistor Values

■ **Second-Order Filter Configuration**

AD22653B can be used like a standard OPAMP. Several filter topologies can be implemented by using AD22653B, both single-ended and differential input configuration, see figure 6. For inverting input configuration, the overall gain is  $-\frac{R2}{R1}$ , the high-pass filter's cutoff frequency is  $\frac{1}{2\pi R1C3}$ , the

low-pass filter's cutoff frequency is  $\frac{1}{2\pi\sqrt{R2R3C1C2}}$ , The detail component values are listed on table

2.

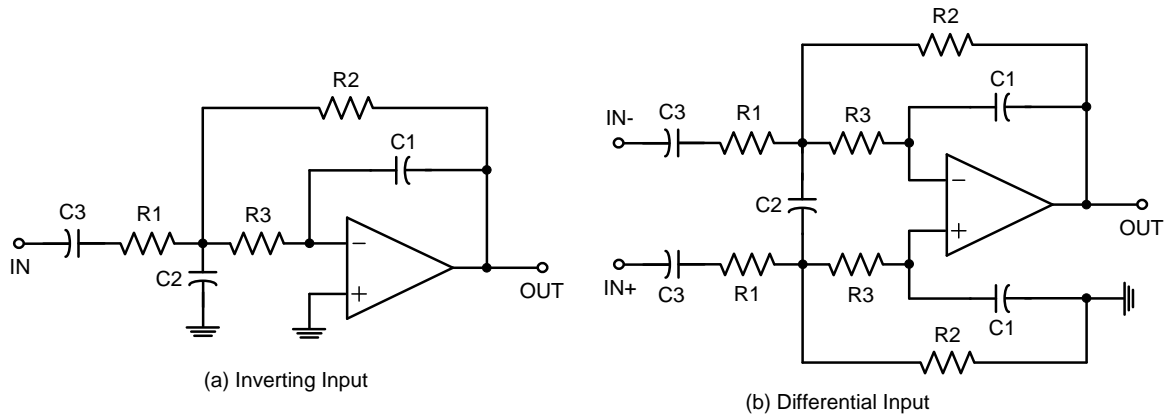


Figure 6. Second-order Active Low-Pass Filter

Gain (V/V)	High Pass (Hz)	Low Pass (kHz)	C1 (pF)	C2 (pF)	C3 (μF)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
-1	1.6	40	100	680	10	10	10	24
-1.5	1.3	40	68	680	15	8.2	12	30
-2	1.6	60	33	150	6.8	15	30	47
-2	1.6	30	47	470	6.8	15	30	43
-3.33	1.2	30	33	470	10	13	43	43
-10	1.5	30	22	1000	22	4.7	47	27

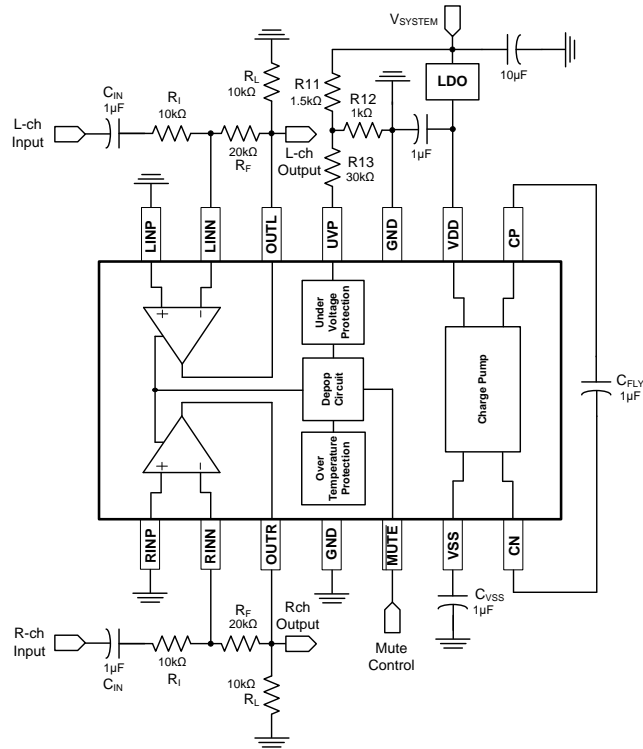
Table 2. Second-order Low-Pass Filter Specifications

■ **Over-Temperature Protection**

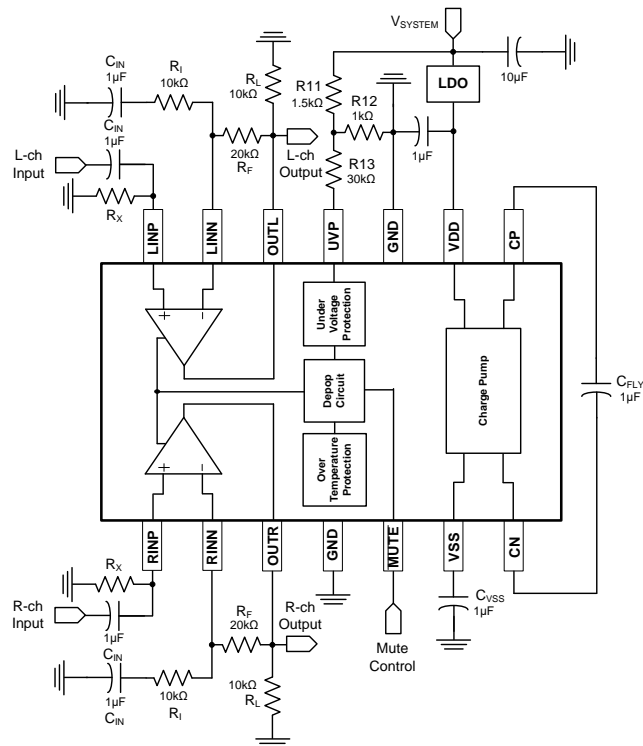
AD22653B provide an over-temperature protection to limit the junction temperature to 150°C. As junction temperature exceeds 150°C, internal thermal sensor will turn off the drivers immediately. The drivers will turn on again if the junction temperature is smaller than 130°C. A 20°C hysteresis is designed to lower the average junction temperature during continuous thermal overload conditions, increasing lifetime of the chip.

## Typical Application Circuit

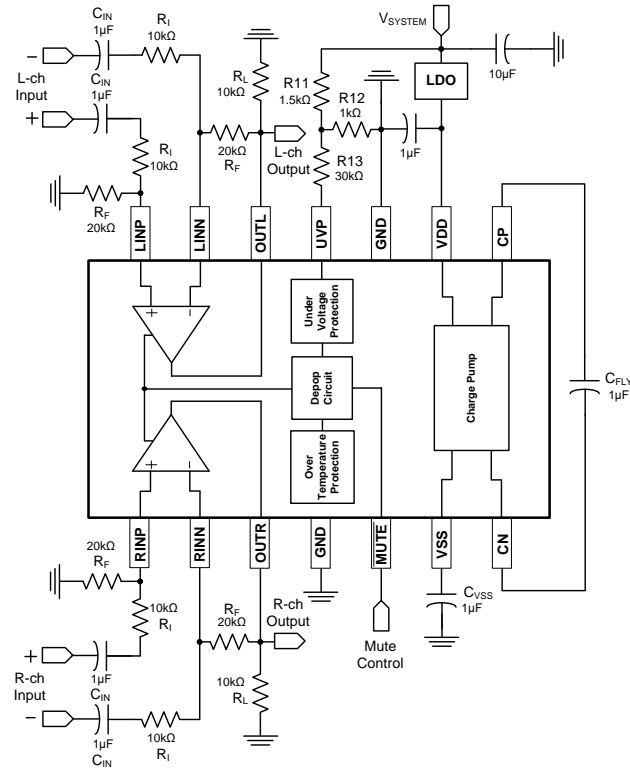
### ■ Inverting Input Line Driver Amplifier



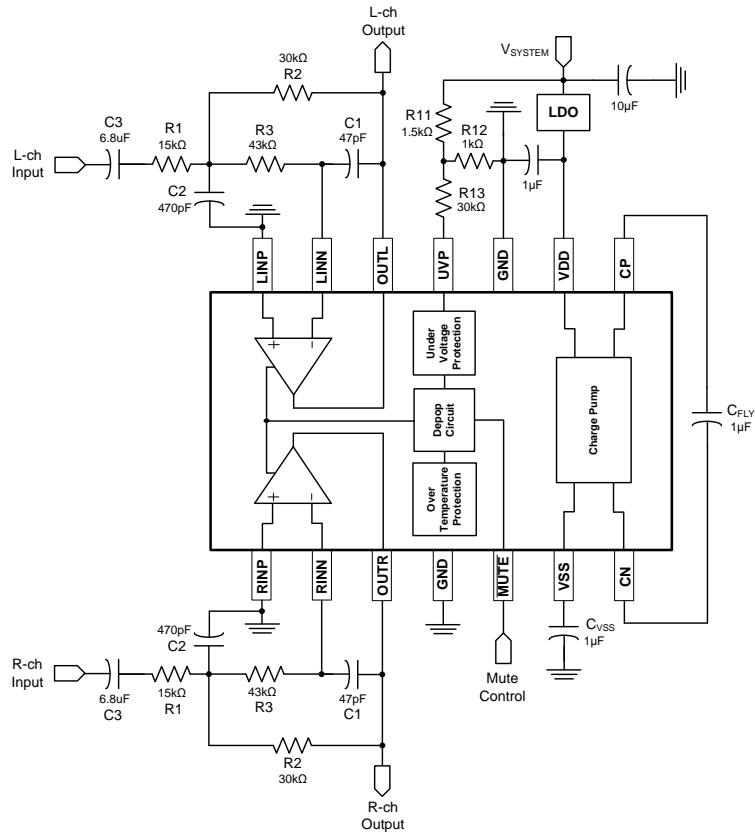
### ■ Non-inverting Input Line Driver Amplifier



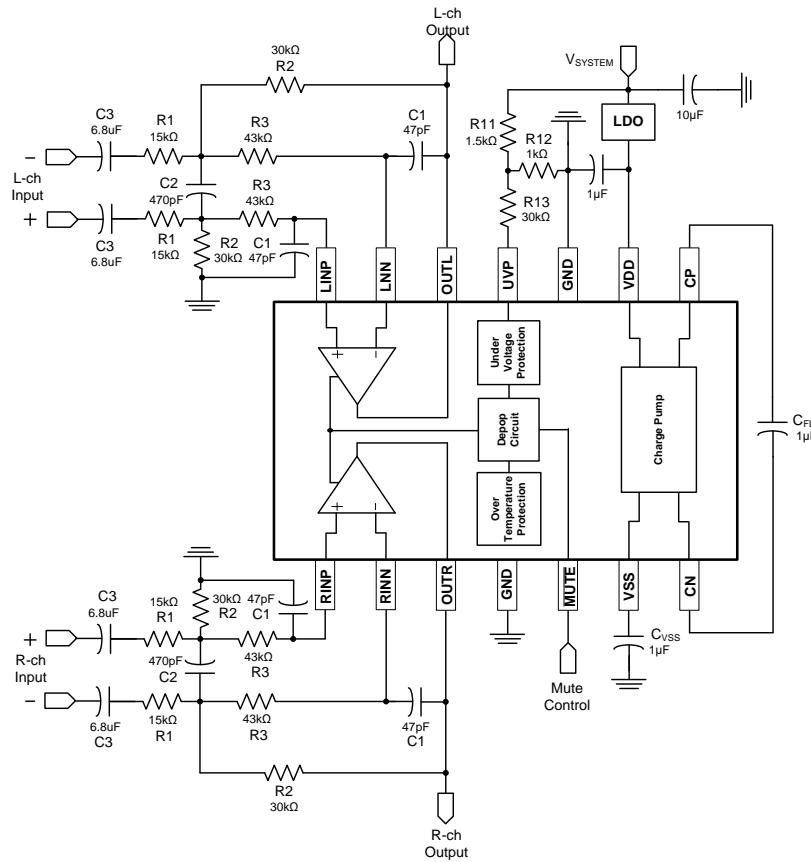
■ **Differential Input Line Driver Amplifier**



■ **Inverting Input Second-Order Active Low-Pass Filter (load support  $\geq 600\Omega$  only)**

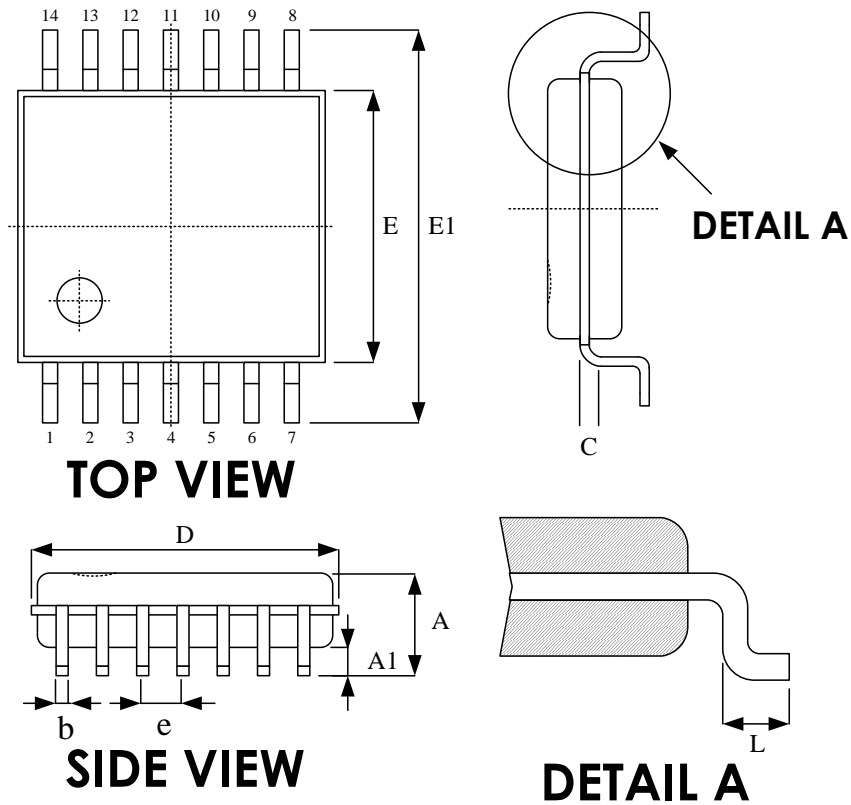


■ **Differential Input Second-Order Active Low-Pass Filter (load support  $\geq 600\Omega$  only)**





**Package Outline Drawing**  
TSSOP-14 (173mil)



Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.16
D	4.90	5.10
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Description</b>
0.1	2014.04.08	Original.
0.2	2014.12.09	Added UVP description to avoid UVP pin test mode trigger.
1.0	2015.03.05	Revise version to 1.0
1.1	2016.02.18	Added UVP description into datasheet.
1.2	2016.03.11	Change minimum load from 600ohm to 16ohm Add 16 data into Electrical Characteristics and Typical Characteristics.
1.3	2018.02.12	Update typical application circuit.
1.4	2018.09.13	Update UVP description.

**Important Notice**

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