Ultra High-PSRR, Low-Noise, 300mA CMOS Linear Regulator

General Description

The EMP8130 features ultra-high power supply rejection ratio, low output voltage noise, low dropout voltage, low quiescent current and fast transient response. It guarantees delivery of 300mA output current and supports preset output voltages ranging from 0.8V to 4.5V with 0.1V increment.

Based on its low quiescent current consumption and its less than 1uA shutdown mode of logical operation, the EMP8130 is ideal for battery-powered applications. The high power supply rejection ratio of the EMP8130 holds well for low input voltages typically encountered in battery-operated systems. The regulator is stable with small ceramic capacitive loads .

The EMP8130 offers current fold-back which throttles down the output current with a decrease in load resistance. The typical value at which current fold-back kicks in is 420mA; the typical value of the output short current limit value is 40mA.

The EMP8130 is available in miniature SOT-23-5, uDFN-4, SOT-23-3 and TDFN-6 package.

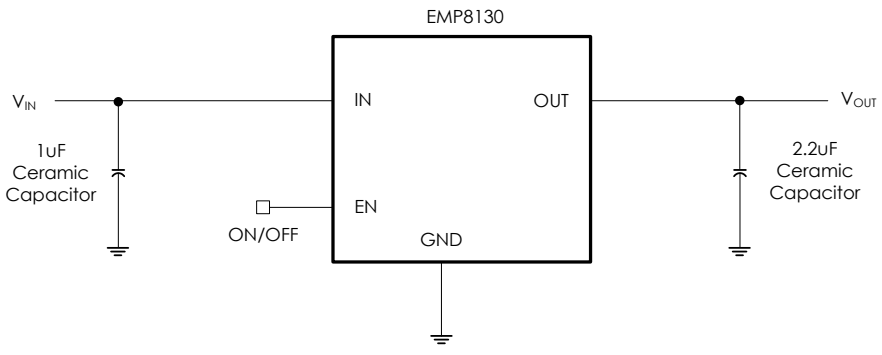
Applications

- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

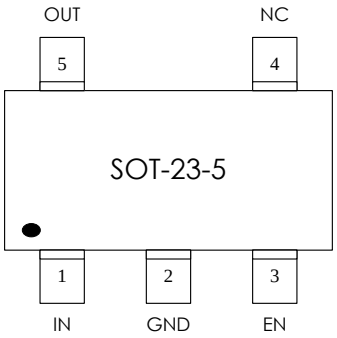
Features

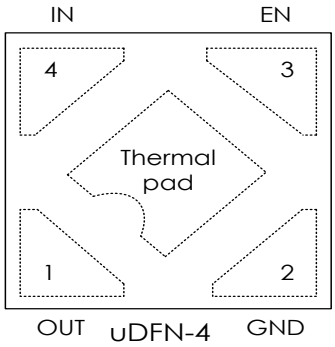
- 300mA guaranteed output current
- 75dB typical PSRR at 1kHz
- 260mV (V_{OUT}=3.3V) typical dropout at 300mA
- 52μA typical quiescent current
- Less than 1μA typical shutdown mode
- Fast line and load transient response
- 1.7V to 5.5V input range
- Auto-discharge during chip disable
- 0.8V to 4.5V output voltage range
- Stable with small ceramic output capacitors
- Fold-back over current protection
- ±1% output voltage tolerance

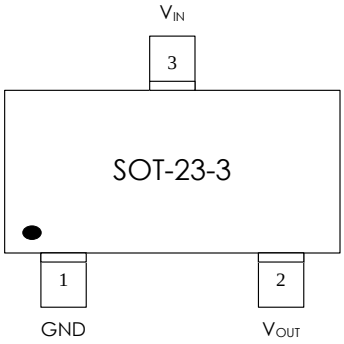
Typical Application

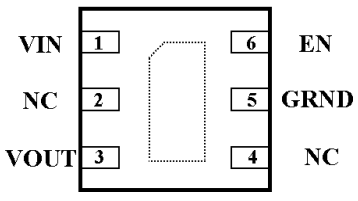


Connection Diagrams









Order information

EMP8130-XXVN05NRR

XX	Output voltage
VN05	SOT-23-5 Package
NRR	RoHS & Halogen free package Rating: -40 to 85°C Package in Tape & Reel

EMP8130-XXFJ04NRR

XX	Output voltage
FJ04	uDFN-4 Package
NRR	RoHS & Halogen free package Rating: -40 to 85°C Package in Tape & Reel

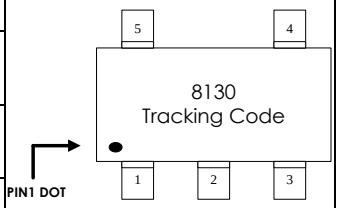
EMP8130-XXVN03NRR

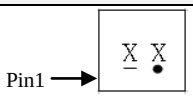
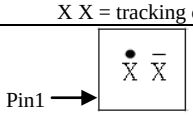
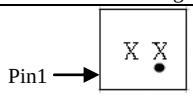
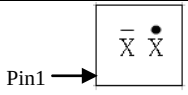
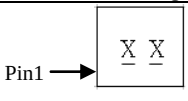
XX	Output voltage
VN03	SOT-23-3 Package
NRR	RoHS & Halogen free package Rating: -40 to 85°C Package in Tape & Reel

EMP8130-XXFK06NRR

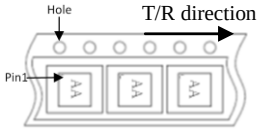
XX	Output voltage
FK06	TDFN-6 Package
NRR	RoHS & Halogen free package Rating: -40 to 85°C Package in Tape & Reel

Order, Marking & Packing Information

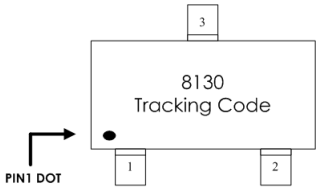
Package	Vout	Product ID.	Marking	Packing
SOT-23-5	0.8V	EMP8130-08VN05NRR (By request)		Tape & Reel 3Kpcs
	1.0V	EMP8130-10VN05NRR		
	1.1V	EMP8130-11VN05NRR		
	1.2V	EMP8130-12VN05NRR		
	1.3V	EMP8130-13VN05NRR (By request)		
	1.5V	EMP8130-15VN05NRR		
	1.8V	EMP8130-18VN05NRR		
	2.5V	EMP8130-25VN05NRR		
	2.7V	EMP8130-27VN05NRR (By request)		
	2.8V	EMP8130-28VN05NRR		
	3.0V	EMP8130-30VN05NRR		
	3.3V	EMP8130-33VN05NRR		

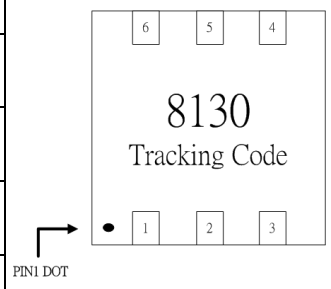
Package	Vout	Product ID.	Marking	Packing
uDFN-4	0.8V	EMP8130-08FJ04NRR (By request)	 X X = tracking code	Tape & Reel 8Kpcs
	1.0V	EMP8130-10FJ04NRR (By request)	 X X = tracking code	
	1.1V	EMP8130-11FJ04NRR (By request)	 X X = tracking code	
	1.2V	EMP8130-12FJ04NRR	 X X = tracking code	
	1.3V	EMP8130-13FJ04NRR (By request)	 X X = tracking code	

	1.5V	EMP8130-15FJ04NRR (By request)	Pin1 → X X X X = tracking code	
	1.8V	EMP8130-18FJ04NRR	Pin1 → X X X X = tracking code	
	2.5V	EMP8130-25FJ04NRR	Pin1 → X X X X = tracking code	
	2.8V	EMP8130-28FJ04NRR	Pin1 → X X X X = tracking code	
	3.0V	EMP8130-30FJ04NRR	Pin1 → X X X X = tracking code	
	3.3V	EMP8130-33FJ04NRR	Pin1 → X X X X = tracking code	



Note : When the hole is located above the tape, the pin1 of the IC is located on the upper left.

Package	Vout	Product ID.	Marking	Packing
SOT-23-3	1.2V	EMP8130-12VN03NRR (By request)		Tape & Reel 3Kpcs
	1.5V	EMP8130-15VN03NRR		
	1.8V	EMP8130-18VN03NRR		
	2.5V	EMP8130-25VN03NRR (By request)		
	2.8V	EMP8130-28VN03NRR		
	3.0V	EMP8130-30VN03NRR		
	3.3V	EMP8130-33VN03NRR		
	4.2V	EMP8130-42VN03NRR (By request)		

Package	Vout	Product ID.	Marking	Packing
TDFN-6	1.2V	EMP8130-12FK06NRR (By request)		Tape & Reel 3Kpcs
	1.8V	EMP8130-18FK06NRR (By request)		
	2.8V	EMP8130-28FK06NRR (By request)		
	3.0V	EMP8130-30FK06NRR (By request)		
	3.3V	EMP8130-33FK06NRR (By request)		

Pin Functions

Name	SOT-23-5	uDFN-4	SOT-23-3	TDFN-6	Function
IN	1	4	3	1	**Supply Voltage Input.** Require a minimum input capacitor of close to 1μF ceramic capacitor to ensure stability and sufficient decoupling from the ground pin.
GND	2	2	1	5	**Ground Pin.**
EN	3	3	N/A	6	**Enable Input.** Enable the regulator by pulling the EN pin High. To keep the regulator on during normal operation, connect the EN pin to V_{IN}. The EN pin must not exceed V_{IN} under all operating conditions.
NC	4	N/A	N/A	2,4	**No Connected.**
OUT	5	1	2	3	**Regulated Output Voltage Pin.** A small 2.2μF ceramic capacitor is needed from this pin to ground to assure stability.
Thermal Pad	N/A	YES	N/A	YES	The thermal pad with large thermal land area on the PCB will helpful chip power dissipation, to connect it to GND together normally.

Functional Block Diagram

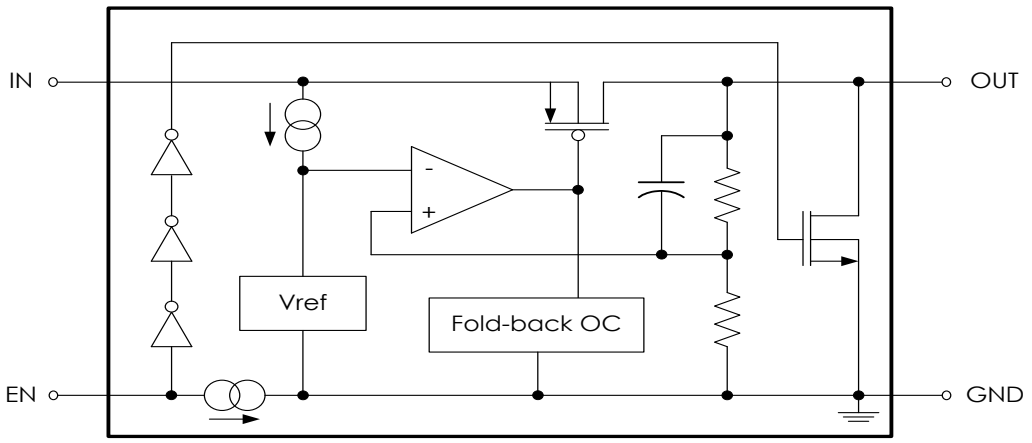


FIG.1. Functional Block Diagram of EMP8130

Absolute Maximum Ratings (Notes 1, 2)

IN, EN, OUT	-0.3V to 6.5V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 6)	ESD Rating	
Storage Temperature Range	-65°C to 150°C	Human Body Model	2KV
Junction Temperature (T_J)	150°C	Machine Model	200V

Operating Ratings (Note 1, 2)

Supply Voltage	1.7V to 5.5V	Operating Temperature Range	-40°C to 85°C

Thermal Resistance:

Symbol	θJA(Note 3)	θJc(Note 4)
SOT-23-5	152(℃/W)	81(℃/W)
uDFN-4	110(℃/W)	23(℃/W)
SOT-23-3	250(℃/W)	81(℃/W)
TDFN-6	165(℃/W)	20(℃/W)

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V (Note 5), V_{EN}=V_{IN}, C_{IN} = 1μF, C_{OUT} =2.2uF, T_A = 25°C. **Boldface** limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
V_{IN}	Input Voltage		**1.7**		**5.5**	V
V_{OUT}	Output Voltage		**0.8**		**4.5**	V
Δ V_{OTL}	Output Voltage Tolerance	Vout>2.0V, T=25	X0.99		X1.01	V
		Vout<=2.0V, T=25	**-20**		**+20**	mV
		Vout>2V, -40~85C	**X0.97**		**X1.03**	V
		Vout<=2V, -40~85C	**-60**		**60**	mV
I_{OUT}	Maximum Output Current	Average DC Current Rating	**300**			mA
I_{cl}	Current Limit	Vin=Vout+1V		420		mA
I_{SC}	Short Current Limit			40		mA
I_Q	Quiescent Current	I_{OUT} = 0mA		52	75	μA
I_{SD}	Shutdown Supply Current	V_{OUT} = 0V, EN = GND		0.2	1	μA
V_{DO}	Dropout Voltage (Note 5)	I_{OUT} = 300mA, Vout=0.8V		860		mV
		I_{OUT} = 300mA, Vout=1.1V		650		
		I_{OUT} = 300mA, Vout=1.2V		580		
		I_{OUT} = 300mA, Vout=1.5V		440		
		I_{OUT} = 300mA, Vout=1.8V		380		
		I_{OUT} = 300mA, Vout=2.8V		290		
		I_{OUT} = 300mA, Vout=3.3V		260		
Δ V_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V		0.02	0.1	%/V
	Load Regulation	1mA ≤ I_{OUT} ≤ 300mA		10	30	mV
PSRR	Power supply rejection ratio	f = 1kHz, Ripple 0.2 Vp-p, Vin=Set Vout +1V, Iout = 30mA		75		dB
e_n	Output Voltage Noise	V_{OUT}=0.8V, I_{OUT}=30mA, 10Hz ≤ f ≤ 100kHz		40		μV_{RMS}
V_{EN}	EN Input Threshold		**1.0**			V

					0.4	
I_{EN}	EN Input Bias Current	EN=GND or VIN		0.1	1	μA

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a high effective thermal conductivity test board (2 layers, 2S0P).

Note 4: θ_{JC} represents the resistance to the heat flows the chip to package top case.

Note 5: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} –V_{OUT} = 1V.

Note 6: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

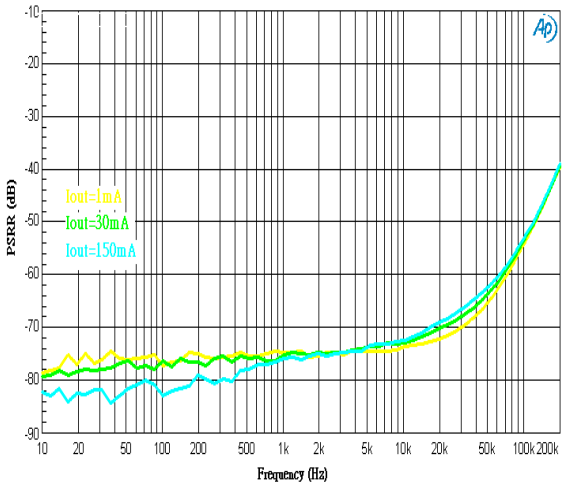
Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the SOT-23-5 packageθ_{JA} = 152°C/W, T_J (MAX) = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 0.82W. The derating factor (-1/θ_{JA}) = -6.6mW/°C, thus below 25°C the power dissipation figure can be increased by 6.6mW per degree, and similarity decreased by this factor for temperatures above 25°C.

Note 7: Typical values represent the most likely parametric norm.

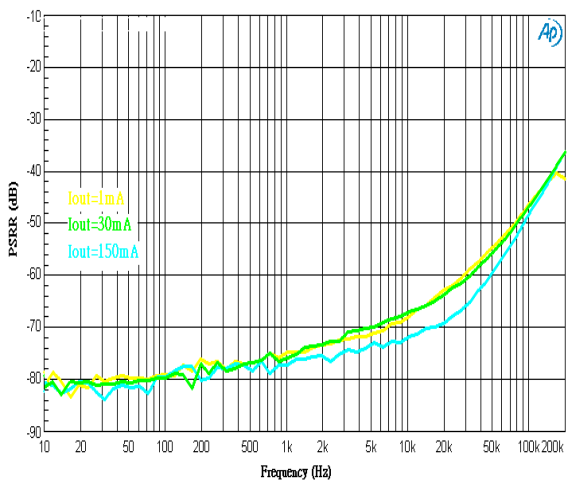
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = 1μF, C_{OUT} =2.2uF, T_A = 25°C

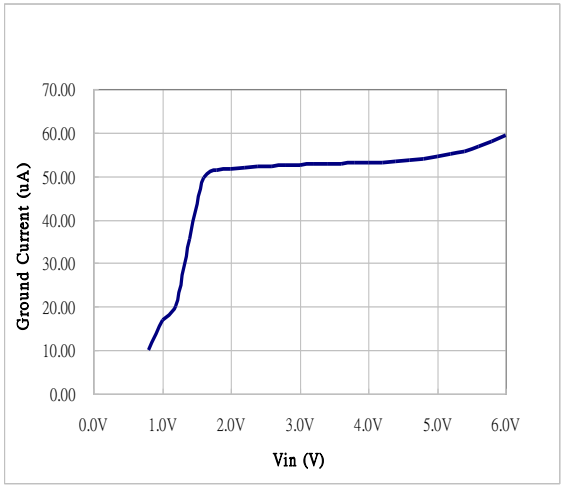
PSRR vs. Frequency (V_{OUT}=0.8V)



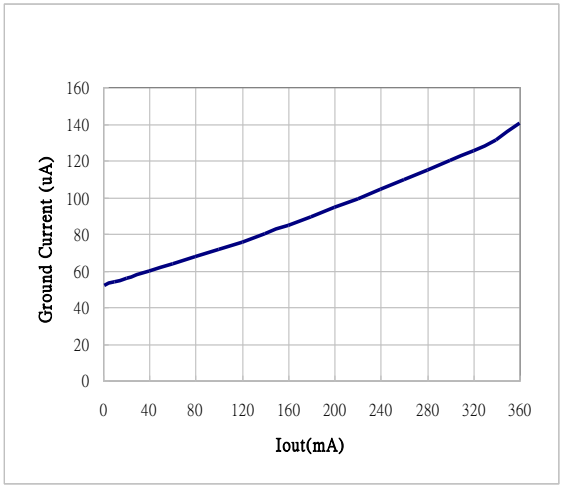
PSRR vs. Frequency (V_{OUT}=3.3V)



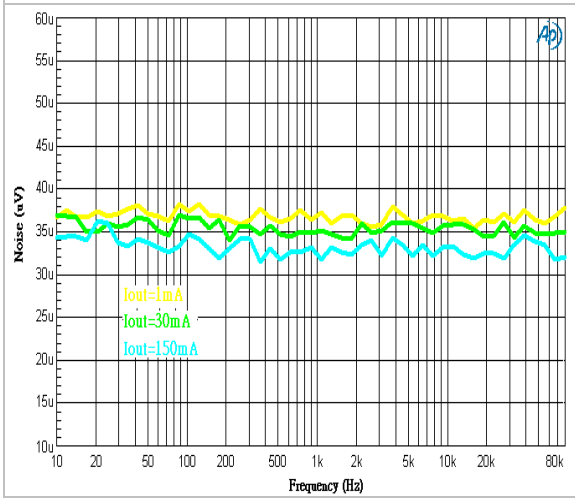
Cround Current vs. V_{IN} (V_{OUT}=0.8V)



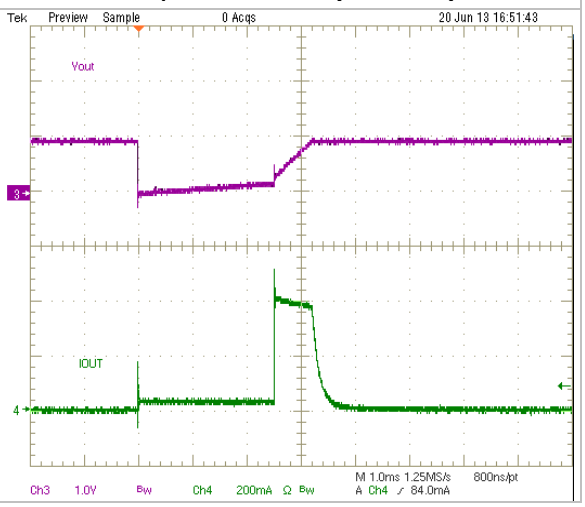
Ground Current vs. I_{OUT} (V_{OUT}=0.8V)



Output Voltage Noise



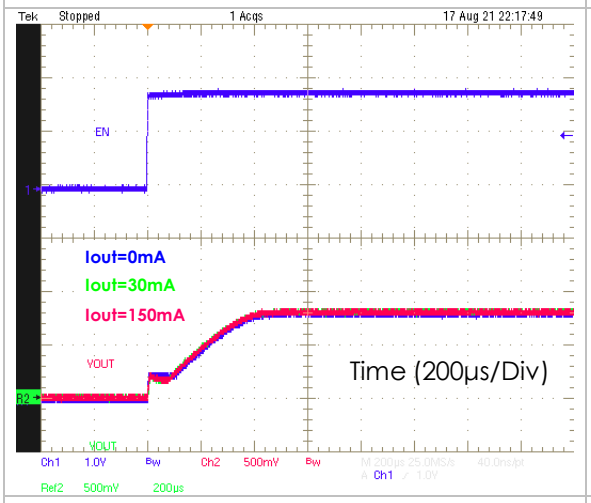
Output Current Limit (Fold-back)



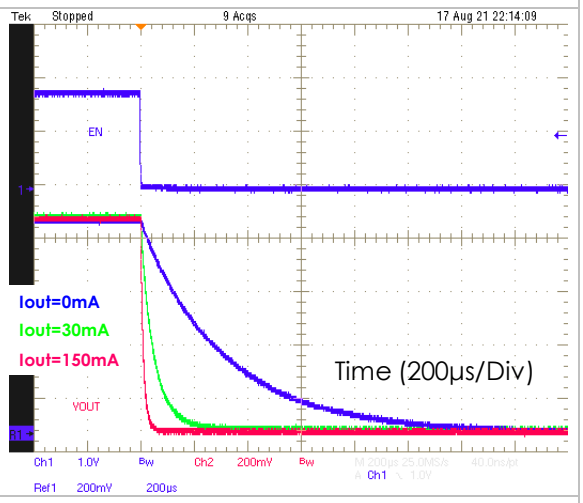
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = 1μF, C_{OUT} =2.2uF, T_A = 25°C

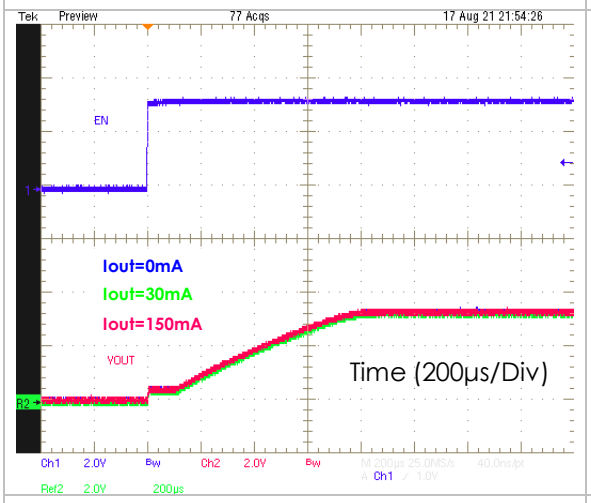
Enable Response (V_{OUT}=0.8V)



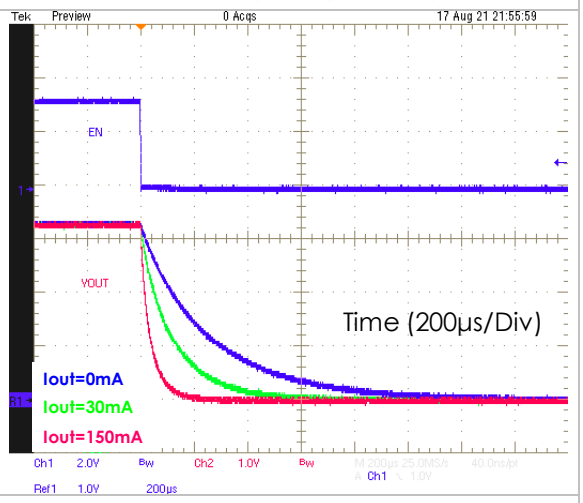
Disable Response (V_{OUT}=0.8V)



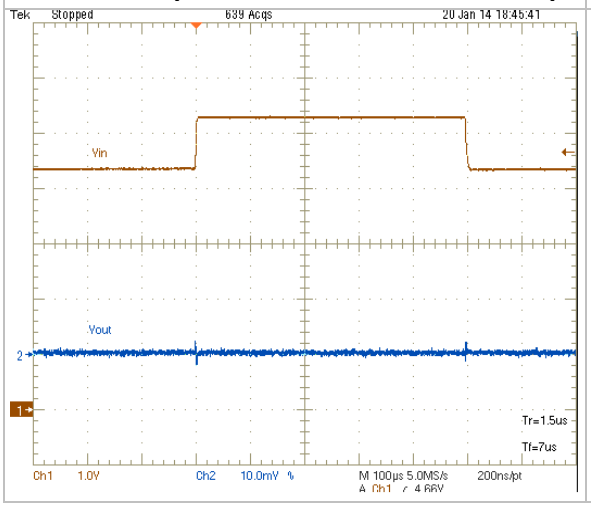
Enable Response (V_{OUT}=3.3V)



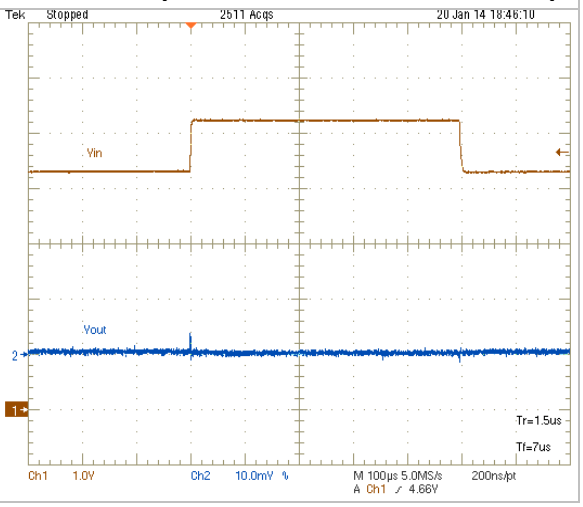
Disable Response (V_{OUT}=3.3V)



Line transient (Iout=30mA,Vin=4.3V~5.3V,V_{OUT}=3.3V)



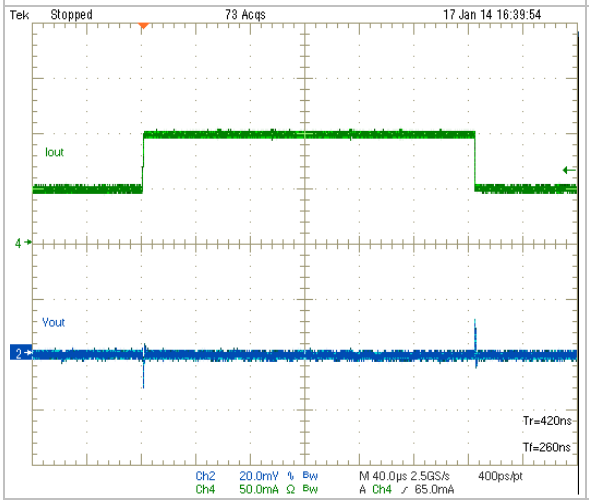
Line transient (Iout=300mA,Vin=4.3V~5.3V,V_{OUT}=3.3V)



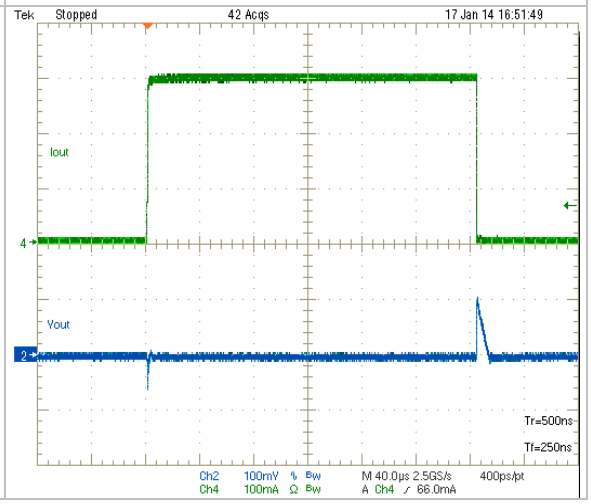
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = 1μF, C_{OUT} =2.2uF, T_A = 25°C

Load transient (V_{OUT}=0.8V, I_{OUT}=50mA to 100mA)



Load transient (V_{OUT}=0.8V, I_{OUT}=1mA to 300mA)



Application Information

General Description

Referring to Fig.1 as shown in the Functional Block Diagram section, the EMP8130 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The sub Vout-select form the feedback circuit which samples the output voltage for the error amplifier's non-inverting input. The inverting input is set to the bandgap reference voltage. Due to its high open-loop gain, the error amplifier ensures that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset voltage reference voltage. The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor, which controls the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register these changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. The regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the temperature and current protection circuitry.

Output Capacitor

The EMP8130 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space, as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8130 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8130 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8130. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA} \times (P_D) + T_A$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$$P_D = I_{OUT} (V_{IN} – V_{OUT})$$

As the above equations show, it is desirable to work with Ics whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8130, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

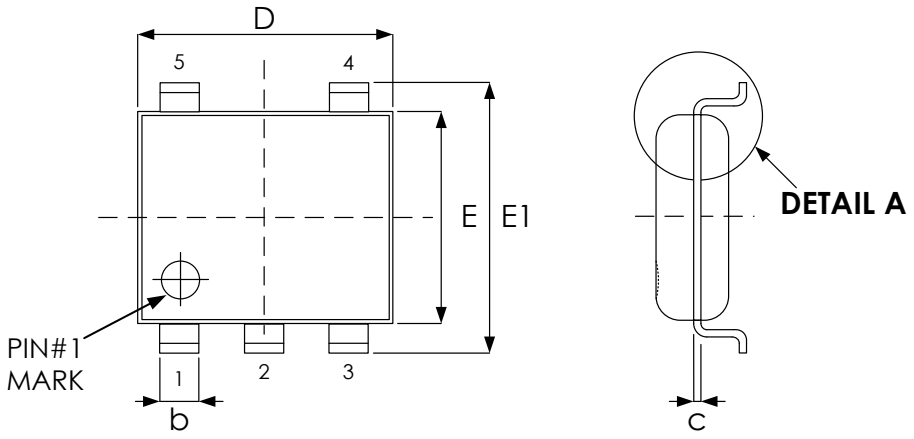
Shutdown

The EMP8130 enters sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically < 1uA. The low supply current makes the EMP8130 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin to enter sleep mode is 0.4V. A minimum guaranteed voltage of 1.0V at the EN pin will activate the EMP8130. To constantly keep the regulator on, direct connection of the EN pin to the VIN pin is allowed.

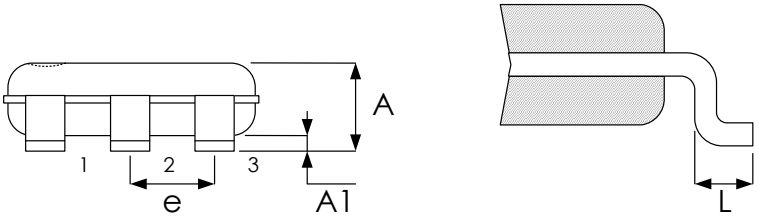
Fold-back Over Current Protection

The EMP8130 has an internal fold-back current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down as the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40mA. Output voltage is not regulated when the device is in current limit, VOUT=ILIMIT x RLOAD. The advantage of fold-back current limit is that the ILIMIT value is less than the fixed current limit. Therefore, the power that the PMOS pass transistor dissipates is much less.

Package Outline Drawing
SOT-23-5



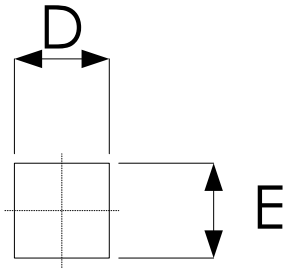
TOP VIEW



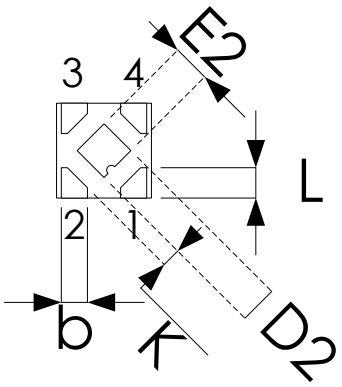
SIDE VIEW **DETAIL A**

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

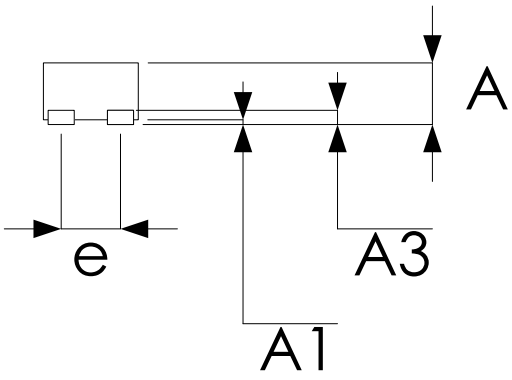
Package Outline Drawing
uDFN-4L (1mmx1 mm)



TOP VIEW



BOTTOM VIEW



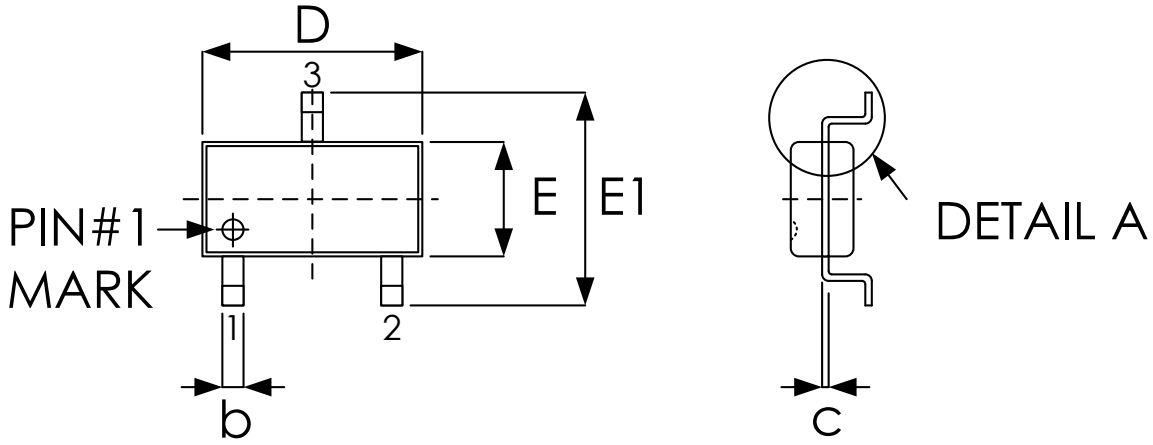
SIDE VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.35	0.60
A1	0.00	0.05
A3	0.12 REF.	
b	0.175	0.275
D	1.00 BSC	
E	1.00 BSC	
e	0.625 BSC	
L	0.200	0.300
K	0.20	-

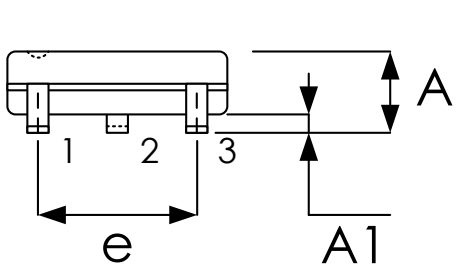
Exposed pad

	Dimension in mm	
	Min	Max
D2	0.40	0.60
E2	0.40	0.60

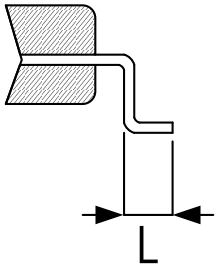
Package Outline Drawing
SOT-23-3



TOP VIEW



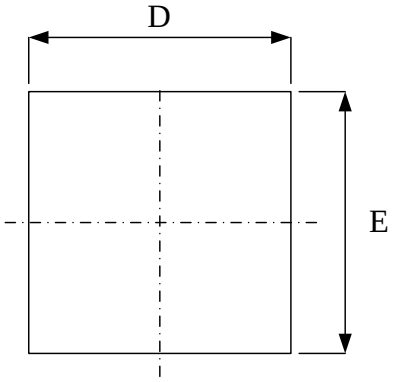
SIDE VIEW



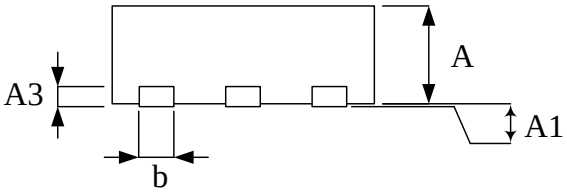
DETAIL A

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	1.90 BSC	
L	0.30	0.60

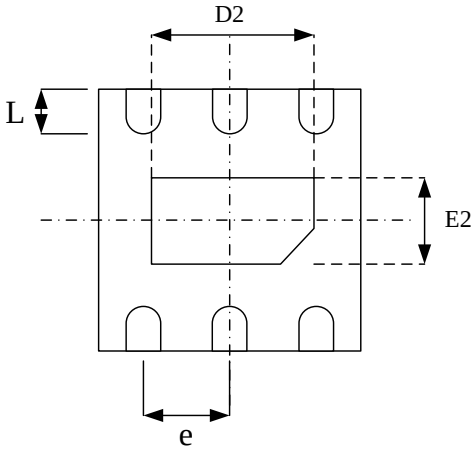
Package Outline Drawing
TDFN-6L (2x2 mm)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.18	0.25
b	0.25	0.35
D	1.90	2.10
E	1.90	2.10
e	0.65 BSC	
L	0.20	0.45

Exposed pad option

	Dimension in mm	
	Min	Max
D2	1.35	1.45
E2	0.55	0.65

Revision History

Revision	Date	Description
0.1	2014.02.11	Initial version.
0.2	2014.05.12	Add uDFN package information
0.3	2014.06.13	Add electrical Characteristics for Icl
0.4	2014.08.22	Add uDFN Thermal Resistance
0.5	2015.01.16	1) Add uDFN PIN number 2) Electrical characteristics format corrected. 3) Add package information SC70 and SC82.
1.0	2015.03.11	Revise version to 1.0 & remove preliminary word
1.1	2015.05.27	Modify connection diagrams and pin functions for uDFN-4
1.2	2015.10.07	Modify application for Output Capacitor(2.2uF)
1.3	2015.11.02	Add TSOT23-5 package information
1.4	2015.11.09	Cancel pin1 dot for uDFN-4 marking
1.5	2016.12.14	Add SOT23-3/TDFN-6 package information
1.6	2017.04.26	Add 2.7V voltage option for SOT23-5 package
1.7	2017.07.31	Add 1.5V/2.5V voltage option for SOT23-3 package
1.8	2017.09.15	Add 1.1V voltage option for SOT23-5 package
1.9	2017.11.14	Add application Information for fold-back current protection
2.0	2017.12.21	1.Update Vout range to 4.5V from 4.0V 2. Add 4.2V voltage option for SOT23-3 package
2.1	2018.01.30	1. Add 1.1V voltage option for uDFN-4 package 2. Add dropout voltage for 1.1V 3.Update uDFN-4 POD
2.2	2020.07.03	1.Remove old order, Marking & Packing Information 2.Add Pin1 location description for UDFN 3.Modify FJ04 package image of Connection Diagrams
2.3	2020.11.19	1.Remove SC70-5,SC82-4 and TSO23-5 package option 2.Add by request for product id
2.4	2021.08.27	Update enable and disable response plots
2.5	2021.09.14	For customer request modify enable and disable response plots.

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.