Flash 3.3V 1 Gbit SPI-NAND Flash Memory

PRODUCT LIST

Parameters	Values
V_{CC}	3.3V
Width	x1, x2[1], x4
Frequency	104MHz
Internal ECC Correction	1-bit
Transfer Rate	9.6ns
Loading Throughput	104MT/s
Power-up Ready Time	1ms (maximum value)
Max Reset Busy Time	1ms (maximum value)

Note: 1. x2 PROGRAM operation is not defined.

FEATURES

- Voltage Supply: 3.3V (2.7V~3.6V)
- Organization
  - Memory Cell Array: (128M + 4M) x 8bit
  - Data Register: (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program: (2K + 64) Byte
  - Block Erase: (128K + 4K) Byte
- Page Read Operation
  - Page Size: (2K + 64) Byte
  - Read from Cell to Register with Internal ECC: 100us
- Memory Cell: 1bit/Memory Cell
- Support SPI-Mode 0 and SPI-Mode 3[1]
- Fast Write Cycle Time
  - Program time:400us
  - Block Erase time: 4ms
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
  - Internal ECC Requirement: 1bit/512Byte
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years
- Command Register Operation
- NOP: 4 cycles
- OTP Operation
- Bad-Block-Protect
- Boot Read

Note: 1. Mode 0: CPOL = 0, CPHA = 0; Mode 3: CPOL = 1, CPHA = 1

ORDERING INFORMATION

Product ID	Speed	Package		Comments
F50L1G41A -104RAG2Y	104MHz	8-contact LGA	8x6mm	Pb-free

GENERAL DESCRIPTION

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non-volatile memory storage solution in systems where pin count must be kept to a minimum. The device is a 1Gb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

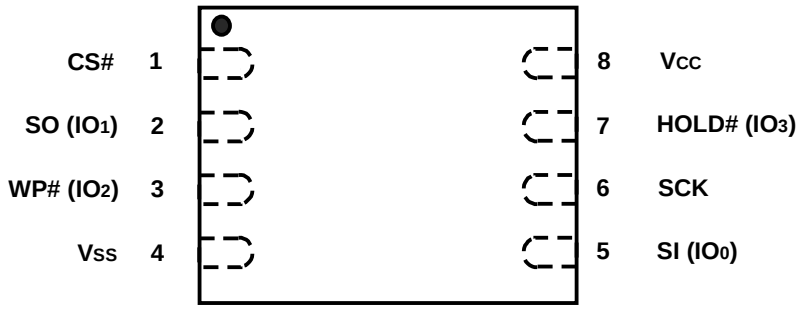
The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. New features include user-selectable internal ECC. With internal ECC enabled, ECC code is generated internally when a page is written to the memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. Each page consists 2112-Byte and is further divided into a 2048-Byte data storage area with a separate 64-Byte spare area. The 64-Byte area is typically used for memory and error management.

The pins serve as the ports for signals. The device has six signal lines plus V_{CC} and ground (GND, V_{SS}). The signal lines are SCK (serial clock), SI (command and data input), SO (response and data output), and control signals CS#, HOLD#, WP#.

PIN CONFIGURATION (TOP VIEW)

8-Contact LGA
(LGA 8C, 8mmx6 mm Body, 1.27mm Contact Pitch)

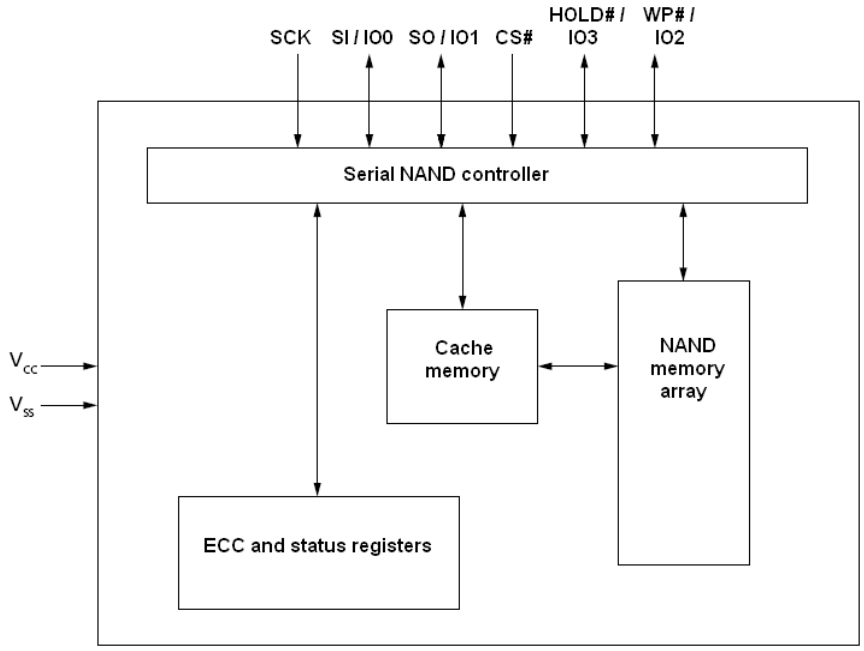


Pin Description

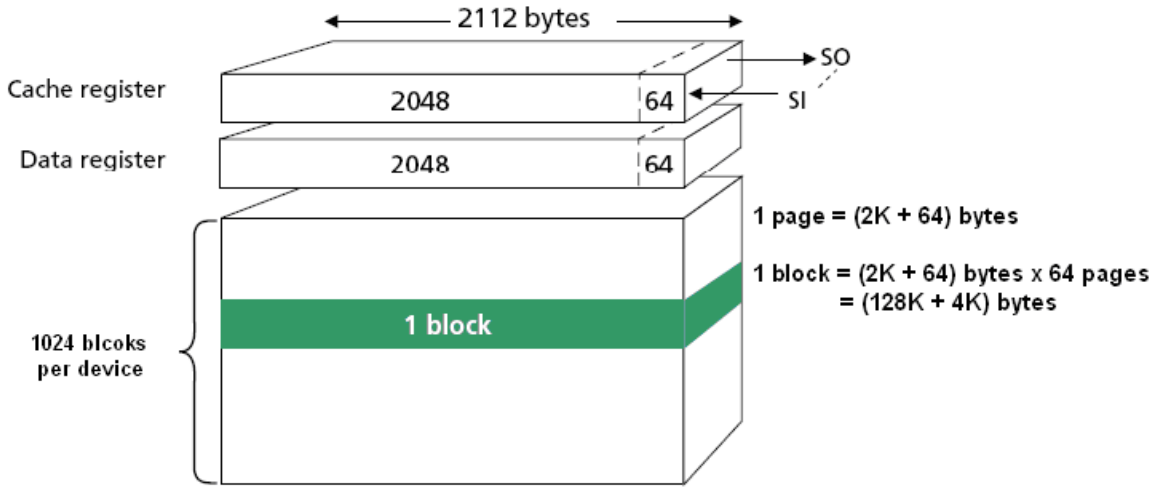
Pin Name	Functions
CS#	**Chip Select (Input)** The device is activated[1]/deactivated[2] as CS# is driven LOW/HIGH. After power-on, the device requires a falling-edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress.
HOLD# / IO_3	**Hold (Input) / IO_3 (Input/Output)** Hold pauses any serial communication with the device without deselecting it[3]. When driven LOW, SO is at high impedance (Hi-Z), and all inputs in SI and SCK are ignored; CS# also should be driven LOW. HOLD# must not be driven during x4 operation.
WP# / IO_2	**Write Protect (Input) / IO_2 (Input/Output)** WP# is driven LOW to prevent overwriting the block-lock bits (BP0, BP1, and BP2) if the block register write disable (BRWD) bit is set[4]. WP# must not be driven during x4 operation.
SCK	**Serial Clock (Input)** SCK provides serial interface timing. Address, commands, and data in SI are latched on the rising edge of SCK. Output (data in SO) is triggered after the falling-edge of SCK. The clock is valid only when the device is active.[5]
SI / IO_0	**Serial Data Input (Input) / IO_0 (Input/Output)** SI transfers data serially into the device. Device latches addresses, commands, and program data in SI on the rising-edge of SCK. SI must not be driven during x2 or x4 READ operation.
SO / IO_1	**Serial Data Output (Output) / IO_1 (Input/Output)** SO transfers data serially out of the device on the falling-edge of SCK. SO must not be driven during x2 or x4 PROGRAM operation.
V_{CC}[6]	**Power** V_{CC} is the power supply for device.
V_{SS}[6]	**Ground**
NC	**No Connection** Not internally connected.

Note:
1. CS# places the device in active power mode.
2. CS# deselects the device and places SO at high impedance.
3. It means HOLD# input doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.
4. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits can't be altered.
5. SI and SO can be triggered only when the clock is valid.
6. Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

BLOCK DIAGRAM



ARRAY ORGANIZATION



Array Address

Data Bits	0	1	2	3	4	5	6	7	Address
1st byte	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Column Address
2nd byte	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	Column Address
3rd byte	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	Row Address
4th byte	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	Row Address
5th byte	*L	*L	*L	*L	*L	*L	*L	*L	Dummy Address

Note:
Column Address: Starting Address of the Register.
*L must be set to “Low”.
The device ignores any additional input of address cycles than required.

COMMAND SET

Function	Op Code	Address Byte	Dummy Byte	Data Bytes
BLOCK ERASE	D8h	3	0	0
GET FEATURE[1]	0Fh	1	0	1
SET FEATURE	1Fh	1	0	1
WRITE DISABLE	04h	0	0	0
WRITE ENABLE	06h	0	0	0
PROGRAM LOAD	02h	2	0	1 to 2112
PROGRAM LOAD x4[2]	32h	2	0	1 to 2112
PROGRAM LOAD RANDOM DATA	84h	2	0	1 to 2112
PROGRAM LOAD RANDOM DATA x4[2]	34h	2	0	1 to 2112
PROGRAM EXECUTE	10h	3	0	0
PAGE READ	13h	3	0	0
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112
READ FROM CACHE x2	3Bh	2	1	1 to 2112
READ FROM CACHE x4[2]	6Bh	2	1	1 to 2112
READ ID[3]	9Fh	1	0	2
RESET	FFh	0	0	0

Note:
1. Refer to Feature Register.
2. Command/Address is 1-bit input per clock period, data is 4-bit input/output per clock period.
3. Address is 00h to get JEDEC ID

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +4.6	V
	V_{IN}	-0.6 to +4.6	
	$V_{I/O}$	-0.6 to V_{CC} + 0.3 (< 4.6)	
Temperature Under Bias	T_{BIAS}	-40 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Short Circuit Current	I_{OS}	5	mA

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(Voltage reference to GND, T_A = 0 to 70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	2.6	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC and Operation Conditions

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	f_C=104MHz, CS#=V_{IL}, I_{OUT}=0mA	-	16	20	mA
	Program	I_{CC2}	-	-	16		
	Erase	I_{CC3}	-	-	16		
Stand-by Current (TTL)		I_{SB1}	CS#=V_{IH}, WP#=0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	CS#= V_{CC} -0.2, WP#=0V/ V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±10	uA
Input High Voltage		V_{IH}[1]	-	0.7 x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL}[1]	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}=-20uA	0.7 x V_{CC}	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=1mA	-	-	0.15 x V_{CC}	V

Note:
1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC}+0.4V for durations of 20ns or less.
2. Typical value are measured at V_{CC} =3.3V, T_A=25℃. Not 100% tested.

Valid Block and Error Management

Description	Requirement
Minimum / Maximum number of valid block number of block	1004 / 1024
Bad block mark	Non FFh
Mark location	Column 2048 of page 0 and page 1

Note:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

AC Test Condition

(T_A=0 to 70℃, V_{CC}=2.7V~3.6V)

Parameter	Condition
Input Pulse Levels	$0.2V_{CC}$ to $0.8V_{CC}$
Input Rise and Fall Times	Max: 2.4ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L=15pF

Capacitance

(T_A=25℃, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

Read / Program / Erase Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Average Program Time	t_{PROG}	-	400	900	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	4	10	ms
Data Transfer from Cell to Register with Internal ECC	t_{RD}	-	-	100	us

General Timing Characteristic

Parameter	Symbol	Min.	Max.
Clock frequency	f_C		104MHz
Hold# non-active hold time relative to SCK	t_{CD}	4.5ns	
Hold# hold time relative to SCK	t_{CH}	4.5ns	
Command deselect time	t_{CS}	100ns	
CS# Setup Time	t_{CSS}	5ns	
CS# Hold Time	t_{CSH}	5ns	
The last valid Clock low to CS# high	t_{CSCL}	5ns	
Output disable time	t_{DIS}		20ns
Hold# non-active setup time relative to SCK	t_{HC}	4.5ns	
Hold# setup time relative to SCK	t_{HD}	4.5ns	
Data input setup time	t_{SUDAT}	2ns	
Data input hold time	t_{HDDAT}	5ns	
Output hold time	t_{HO}	2ns	
Hold# to output Hi-Z	t_{HZ}		7ns
Hold# to output Low-Z	t_{LZ}		7ns
Clock low to output valid	t_V		8ns
Clock high time	t_{WH}	4.5ns	
Clock low time	t_{WL}	4.5ns	
Clock rise time (slew rate)	t_{CRT}	0.1V/ns	
Clock fall time (slew rate)	t_{CFT}	0.1V/ns	
WP# setup time	t_{WPS}	20ns	
WP# hold time	t_{WPH}	100ns	
Resetting time during Idle/Read/Program/Erase	t_{RST}		5/5/10/500us

Note: For first RESET condition after power up, t_{RST} will be 1ms MAX.

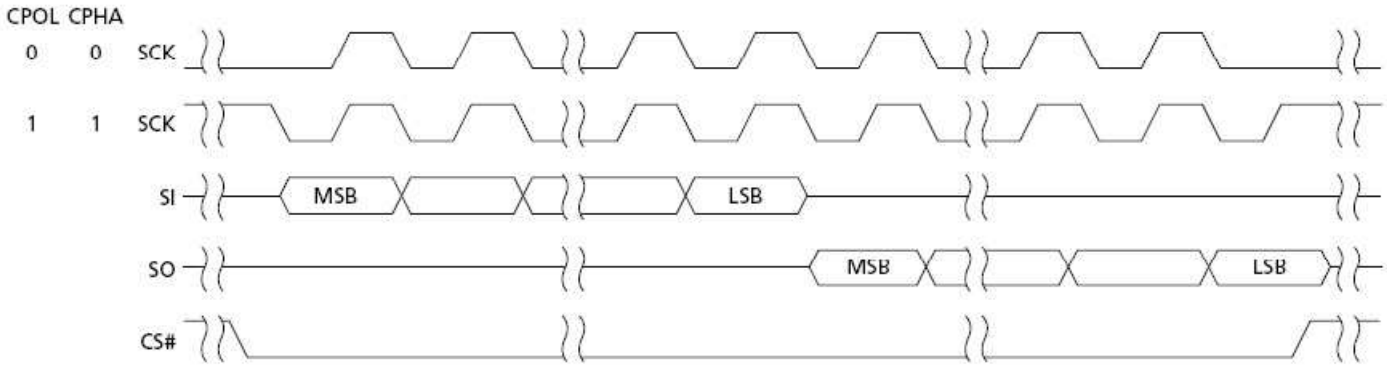
Technical Notes

Bus Operation

SPI NAND supports two SPI modes:
(Mode 0) CPOL (clock polarity) = 0, CPHA (clock phase) = 0
(Mode 3) CPOL=1, CPHA=1

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.
When CS# is high, keep SCK at V_{CC} (Mode 0) or V_{SS} (Mode 3). Do not begin toggling SCK until after CS# is driven LOW.

SPI Modes Timing



Feature Operations

The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-Byte feature address to determine which feature is to be read or modified.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in Feature Setting Table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Feature Settings Table

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock[1]	A0h	BRWD	Reserved	BP2	BP1	BP0	Reserved	Reserved	Reserved
OTP	B0h	OTP Protect	OTP Enable	Reserved	ECC Enable[2]	Reserved	Reserved	Reserved	Reserved
Status	C0h	Reserved	Reserved	ECC_S1	ECC_S0	P_Fail	E_Fail	WEL[3]	OIP
Output Driver	D0h[4]	Reserved	DRV_S1	DRV_S0	Reserved	Reserved	Reserved	Reserved	Reserved

Note:
1. 38h is the default data byte value for Block Lock Register after power-up.
2. 1-bit internal ECC for all READ and PROGRAM operations can be enabled (ECC enable = 1) or disabled (ECC enable = 0); (10h) is the default data byte value for OTP Register after power-up.
3. WEL = 0 is the default data bit value for Status Register after power-up.
4. (20h) is the default data byte value for Output Driver Register after power-up.

Block Protect Bits of Block Lock Register Table

BP2 (5)	BP1 (4)	BP0 (3)	Protected Rows
0	0	0	None; all unlocked
0	0	1	Upper 1/64 locked
0	1	0	Upper 1/32 locked
0	1	1	Upper 1/16 locked
1	0	0	Upper 1/8 locked
1	0	1	Upper 1/4 locked
1	1	0	Upper 1/2 locked
1	1	1	All locked (default)

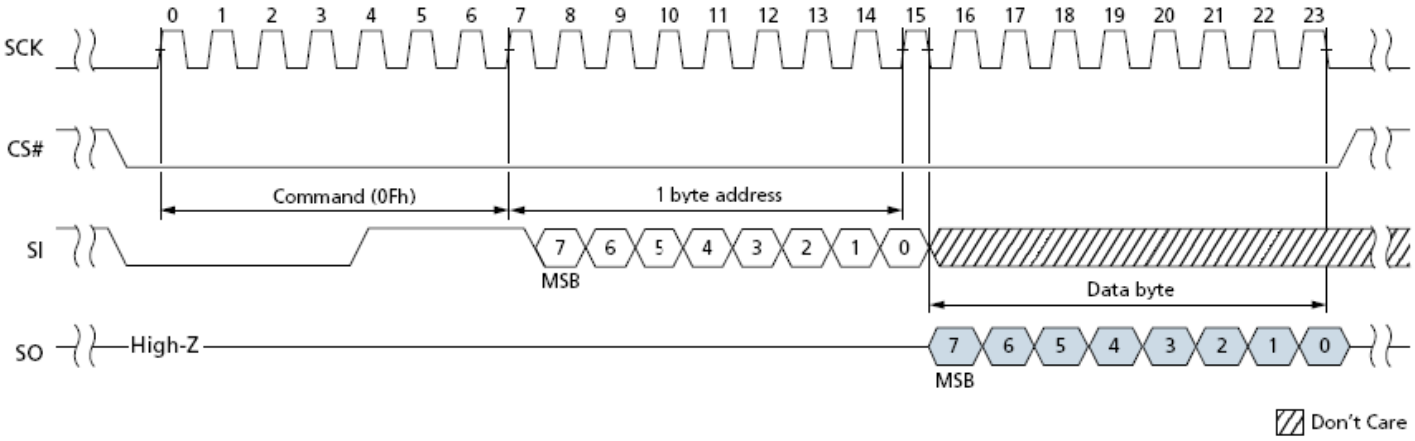
OTP State Bits of OTP Register Table

OTP Protect Bit (7)	OTP Enable Bit (6)	State
0	0	Normal operation (read array)
0	1	Access OTP space
1	0	Not applicable
1	1	Lock the OTP area

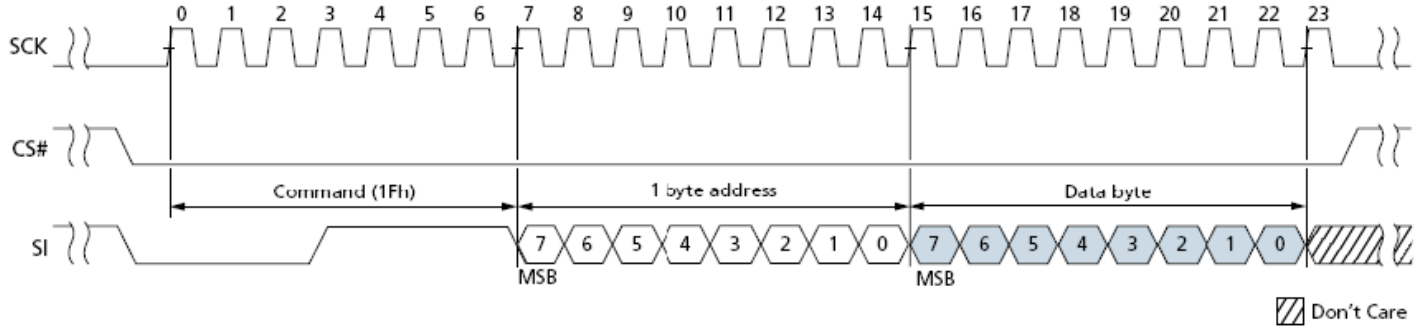
Driver Strength Bits of Output Driver Register Table

DRV_S1	DRV_S0	Driver Strength
0	0	100 %
0	1	75 %
1	0	50 %
1	1	25%

GET FEATURE (0Fh) Timing



SET FEATURE (1Fh) Timing

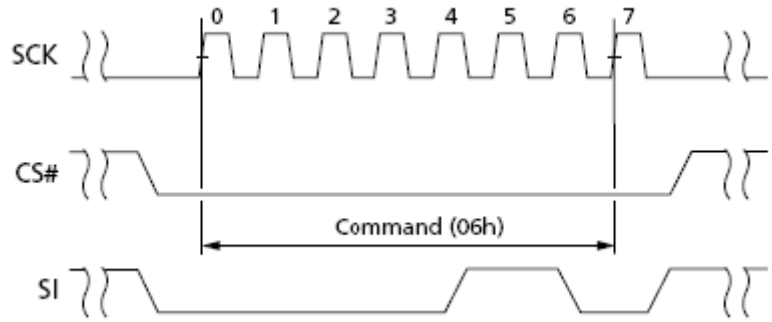


Array Write Enable / Disable

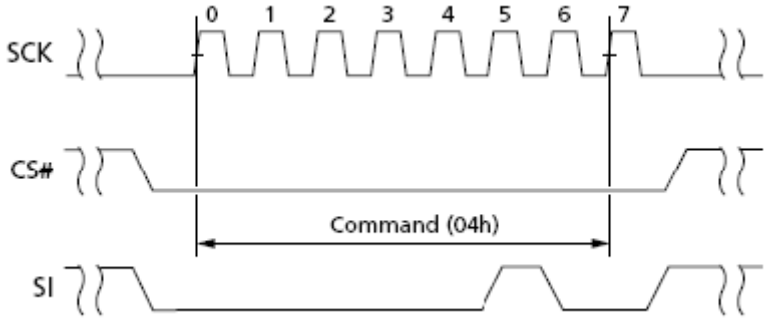
The WRITE ENABLE (06h) command sets the WEL bit (in status register) to 1. This is required in the following WRITE operations that change the contents of the memory array: PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

Contrarily, the WRITE DISABLE (04h) command sets the WEL bit to 0. This disables PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

WRITE ENABLE (06h) Timing



WRITE DISABLE (04h) Timing



Status Register

Software can read status register during the NAND device operation by issuing GET FEATURE (0Fh) command, followed by the feature address C0h. The status register will output the status of the operation, refer to Feature Setting Table, Bits of Status Register Table and ECC Status Bits of Status Register Table.

Bits of Status Register Table

Bit Name	Mode	Description
Program fail (Bit 3)	R	P_Fail is set to 1 as a program failure has occurred. P_Fail = 1 will also be set if the user attempts to program an invalid address or a locked region. P_Fail is set to 0 during the PROGRAM EXECUTE command sequence or the RESET command.
Erase fail (Bit 2)	R	E_Fail is set to 1 as an erase failure has occurred. E_Fail = 1 will also be set if the user attempts to erase a locked region, or if ERASE operation fails. E_Fail is set to 0 at the start of the BLOCK ERASE command sequence or the RESET command.
Write enable latch (Bit 1)	W	WEL must be set to 1 to indicate the current status of the write enable latch, prior to issuing PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing WRITE ENABLE command. WEL is disabled (WEL=0) by issuing the WRITE DISABLE command.
Operation in progress (Bit 0)	R	OIP is set to 1 when the device is busy; it means a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing. OIP is cleared to 0 as the interface is in ready state.
ECC_status1 (Bit 5) ECC_status0 (Bit 4)	R	ECC Status Bits of Status Register Table shows the ECCS definitions. ECC_S is set to 00h either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC_S is invalid if ECC is disabled (via a SET FEATURE command to Bit 4 in OTP register). After power-up RESET, ECC_S is set to reflect the contents of block 0, page 0.

ECC Status Bits of Status Register Table

ECCS1 (5)	ECCS0 (4)	Description
0	0	No errors
0	1	1-bit error detected and corrected
1	0	2-bit errors detected and not corrected
1	1	Reserved

Error Management

Mask Out Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ESMT. The information regarding the initial invalid blocks is called the initial invalid block information. Devices with initial invalid blocks have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block does not affect the performance of valid blocks because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid blocks via address mapping.

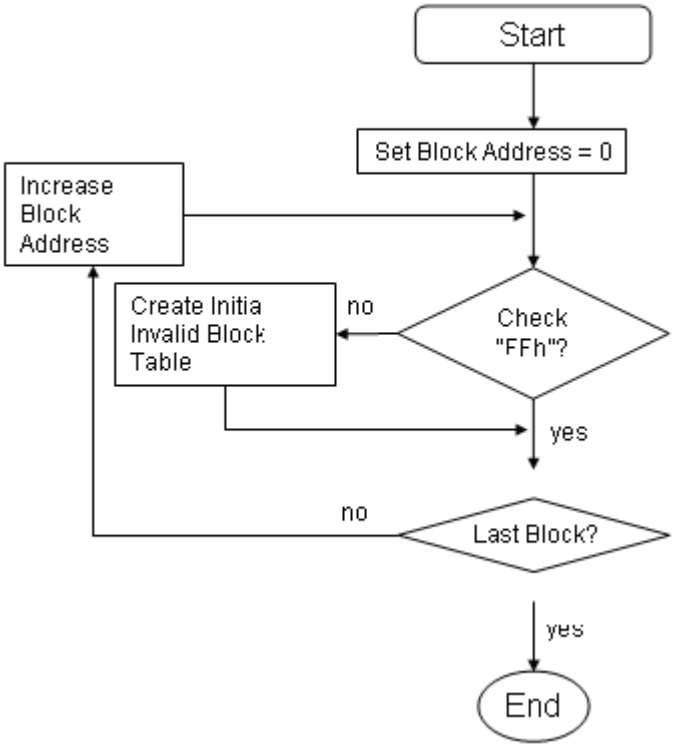
The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

Identifying Initial invalid Blocks

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. ESMT makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the 1st byte column address in the spare area.

Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.

Algorithm for Bad Block Scanning



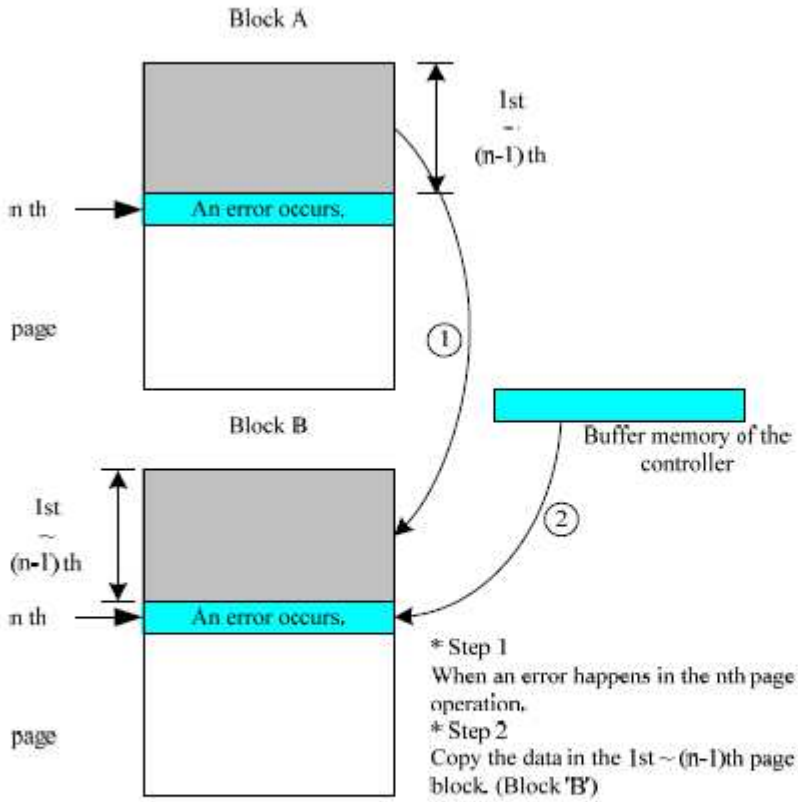
Check “FFh” at the 1st Byte column address in the spare area of the 1st and 2nd page in the block.

```
For (i=0; i<Num_of_LUs; i++)
{
        For (j=0; j<Blocks_Per_LU; j++)
        {
                Defect_Block_Found=False;

                Read_Page(lu=i, block=j, page=0);
                If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)    Defect_Block_Found=True;

                Read_Page(lu=i, block=j, page=1);
                If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)    Defect_Block_Found=True;

                If (Defect_Block_Found)         Mark_Block_as_Defective(lu=i, block=j);
        }

}
```

Block Replacement

Within its lifetime, number of invalid blocks may increase with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of failure after ERASE or PROGRAM in status register, block replacement should be done. Because PROGRAM status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

In case of READ, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.



* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

ECC Protection

ECC is enabled after device power-up, so the default PROGRAM and READ commands operate with internal ECC in the active state. During a PROGRAM operation, the device calculates an ECC code on the 2KB page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page in array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a single-bit data error is discovered, the error is corrected in the cache register and only the corrected data is on the output bus.

ECC Protection Table

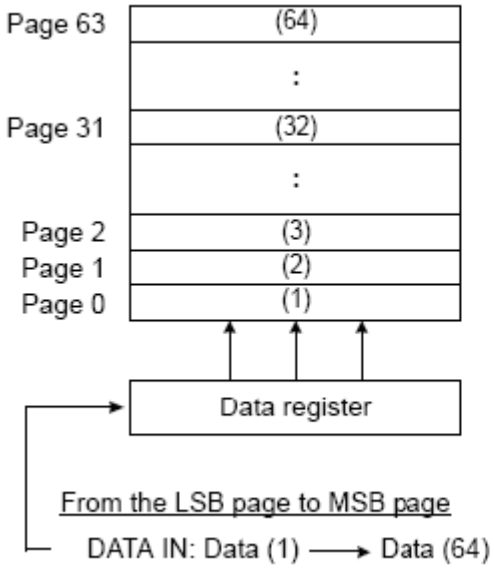
Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh (511)	000h (0)	Yes	Main 0	User data 0[1]
3FFh (1023)	200h (512)	Yes	Main 1	User data 1[1]
5FFh (1535)	400h (1024)	Yes	Main 2	User data 2[1]
7FFh (2047)	600h (1536)	Yes	Main 3	User data 3[1]
800h (2048)	800h (2048)	No		Reserved
803h (2051)	801h (2049)	No		ECC for main 0[2]
807h (2055)	804h (2052)	Yes		ECC for spare 0[2]
80Fh (2063)	808h (2056)	Yes	Spare 0	User meta data 0[1]
810h (2064)	810h (2064)	No		Reserved
813h (2067)	811h (2065)	No		ECC for main 1[2]
817h (2071)	814h (2068)	Yes		ECC for spare 1[2]
81Fh (2079)	818h (2072)	Yes	Spare 1	User meta data 1[1]
820h (2080)	820h (2080)	No		Reserved
823h (2083)	821h (2081)	No		ECC for main 2[2]
827h (2087)	824h (2084)	Yes		ECC for spare 2[2]
82Fh (2095)	828h (2088)	Yes	Spare 2	User meta data 2[1]
830h (2096)	830h (2096)	No		Reserved
833h (2099)	831h (2097)	No		ECC for main 3[2]
837h (2103)	834h (2100)	Yes		ECC for spare 3[2]
83Fh (2111)	838h (2104)	Yes	Spare 3	User meta data 3[1]

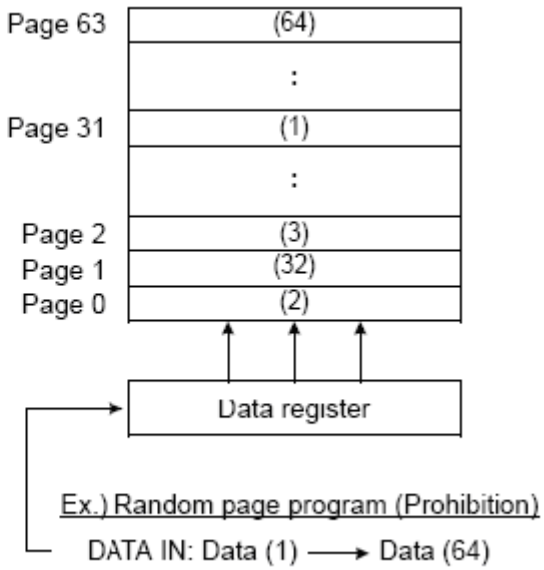
Note:

1. The user areas must be programmed within a single partial-page programming operation so the NAND Flash device can calculate the proper ECC bytes.
2. When internal ECC is enabled, these areas are prohibited to be programming.

Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.





Operations and Timing Diagrams

Read Operations and Serial Output

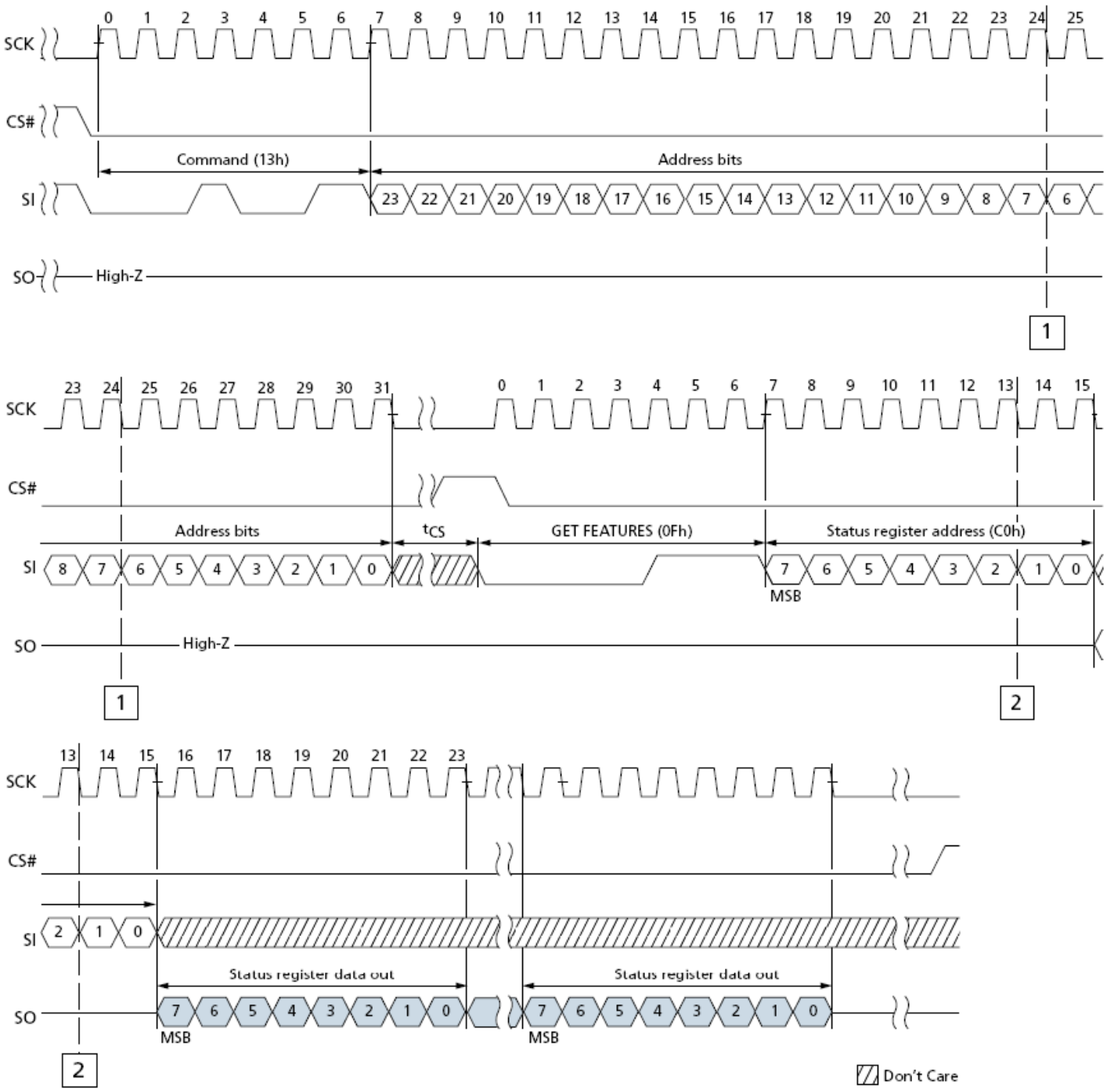
The command sequence is follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURE command to read the status)
- 0Bh or 03h (READ FROM CACHE x1) / 3Bh (x2) / 6Bh (x4)

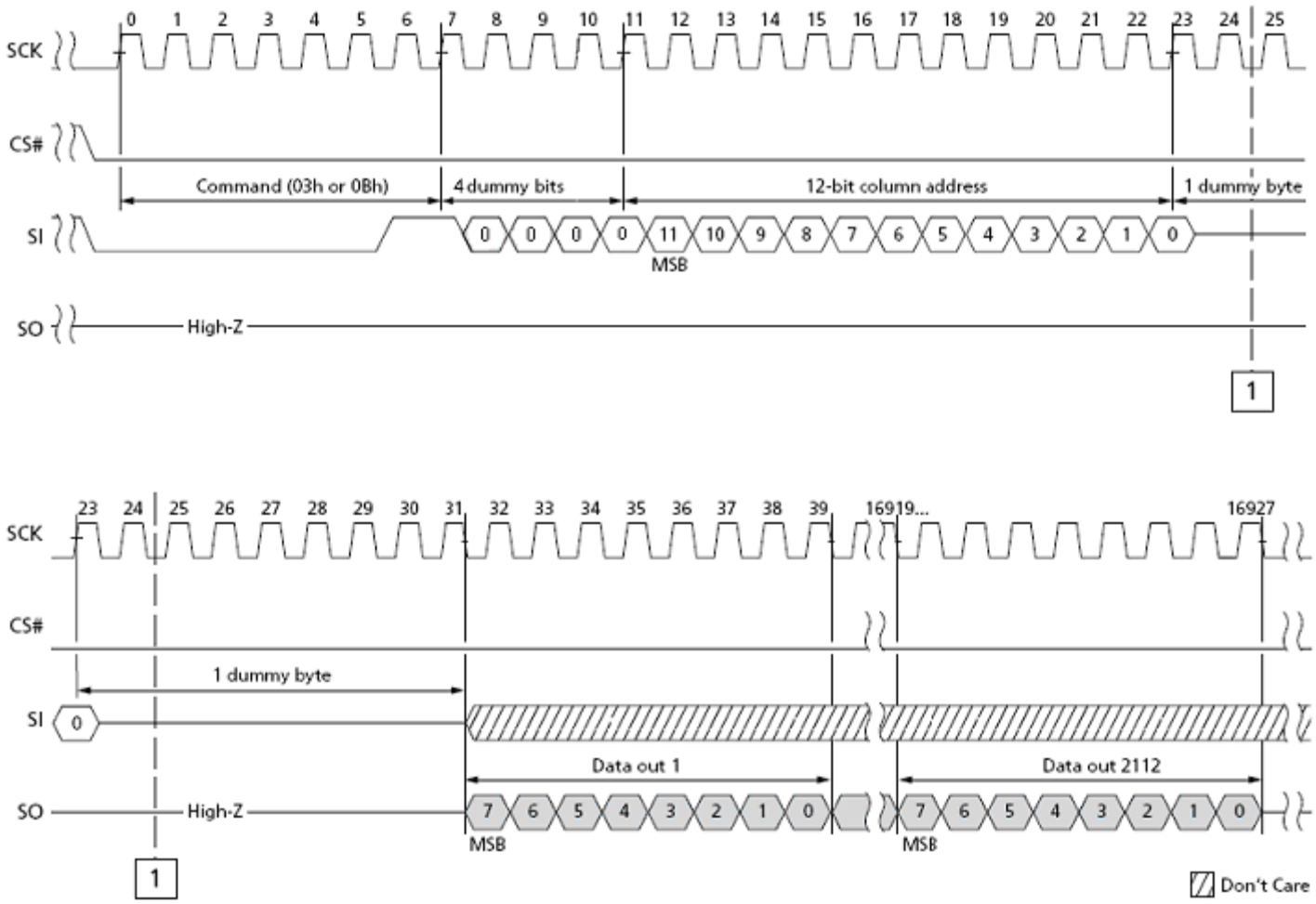
PAGE READ command requires 24-bit address with 8 dummy and a 16-bit row address. After row address is registered, the device starts the transfer from the main array to the cache register, and is busy for t_R time. During this time, GET FEATURE command can be issued to monitor the status of the operation. Following a status of successful completion, READ FROM CACHE command must be issued to read the data out of the cache.

READ FROM CACHE command requires 16-bit address with 4 dummy bits and a 12-bit column address for the starting byte. The starting byte can be 0 to 2011, but after the end of the cache register is reached, the data does not wrap around and SO goes to a Hi-Z state.

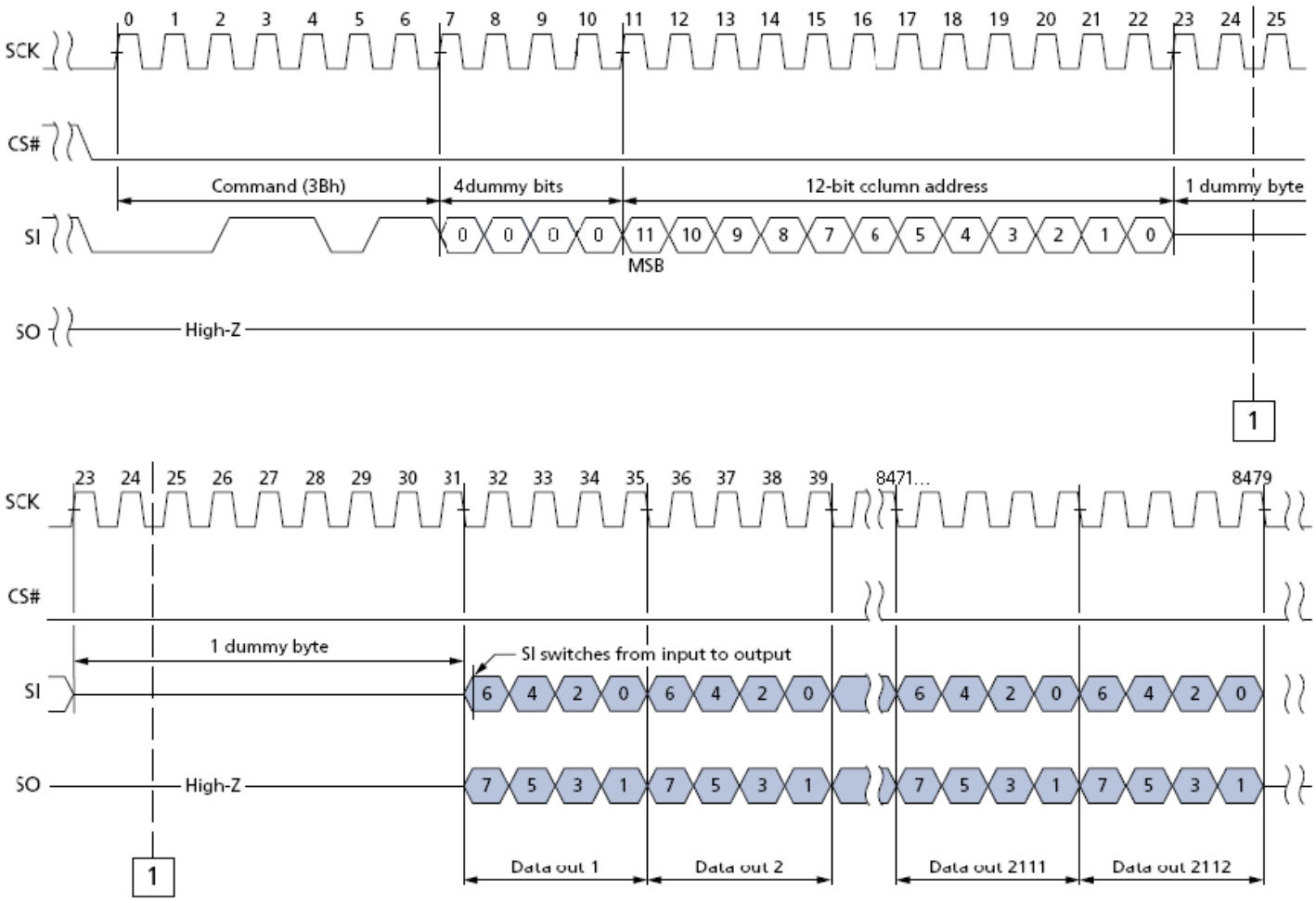
PAGE READ (13h) Timing



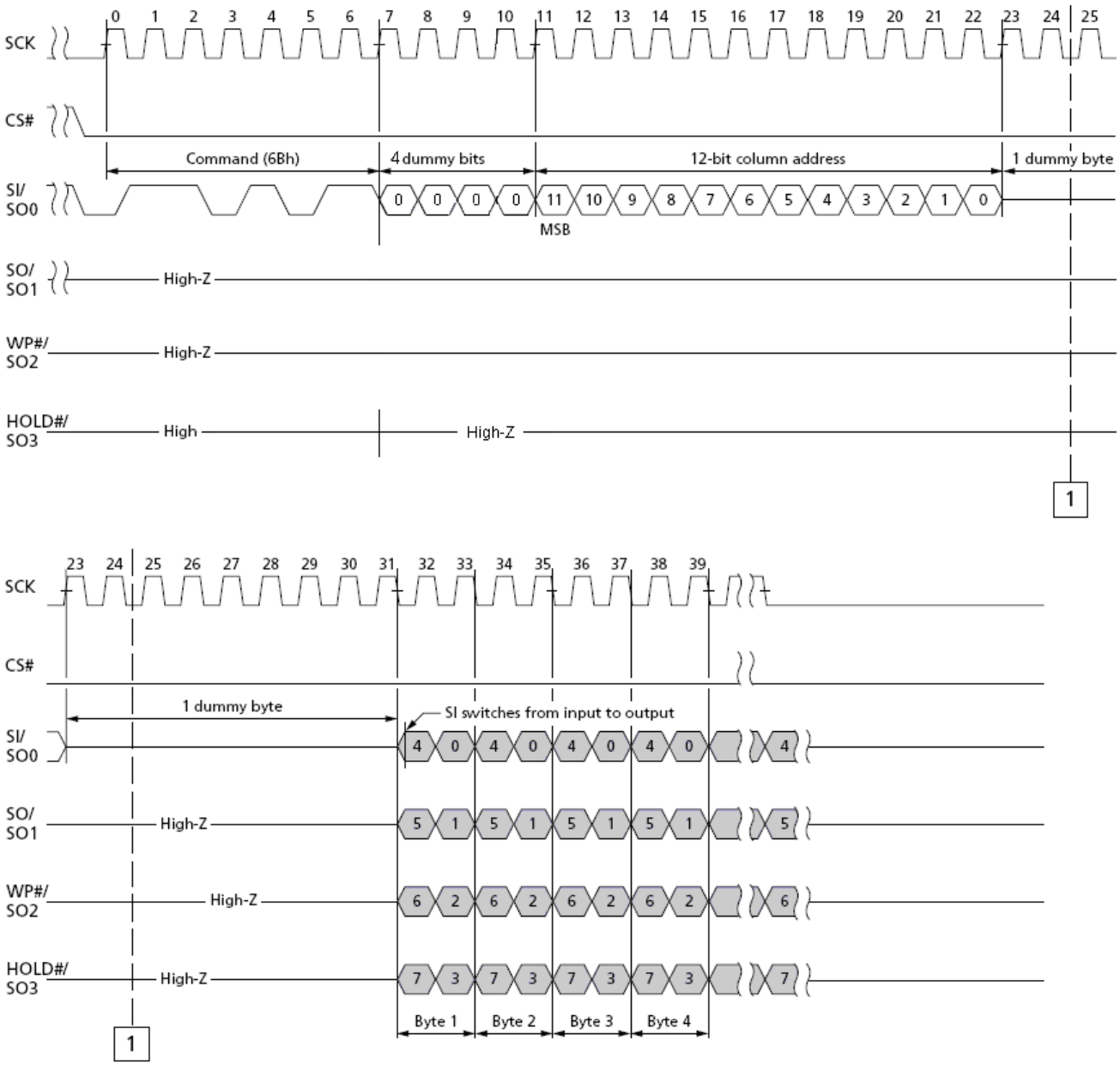
READ FROM CACHE (03h or 0Bh) Timing



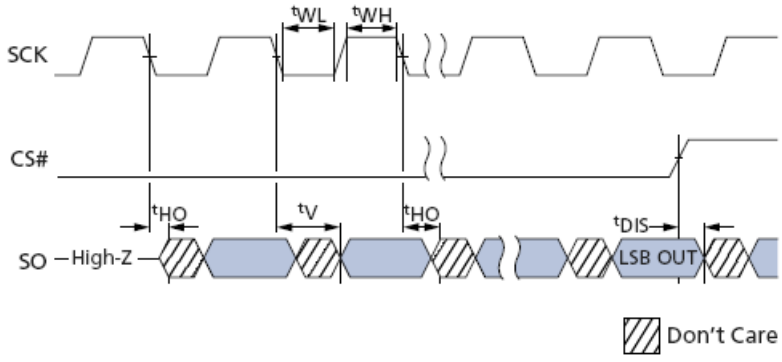
READ FROM CACHE x2 (3Bh) Timing



READ FROM CACHE x4 (6Bh) Timing



Serial Output Timing



Program Operations and Serial Input

Page Program

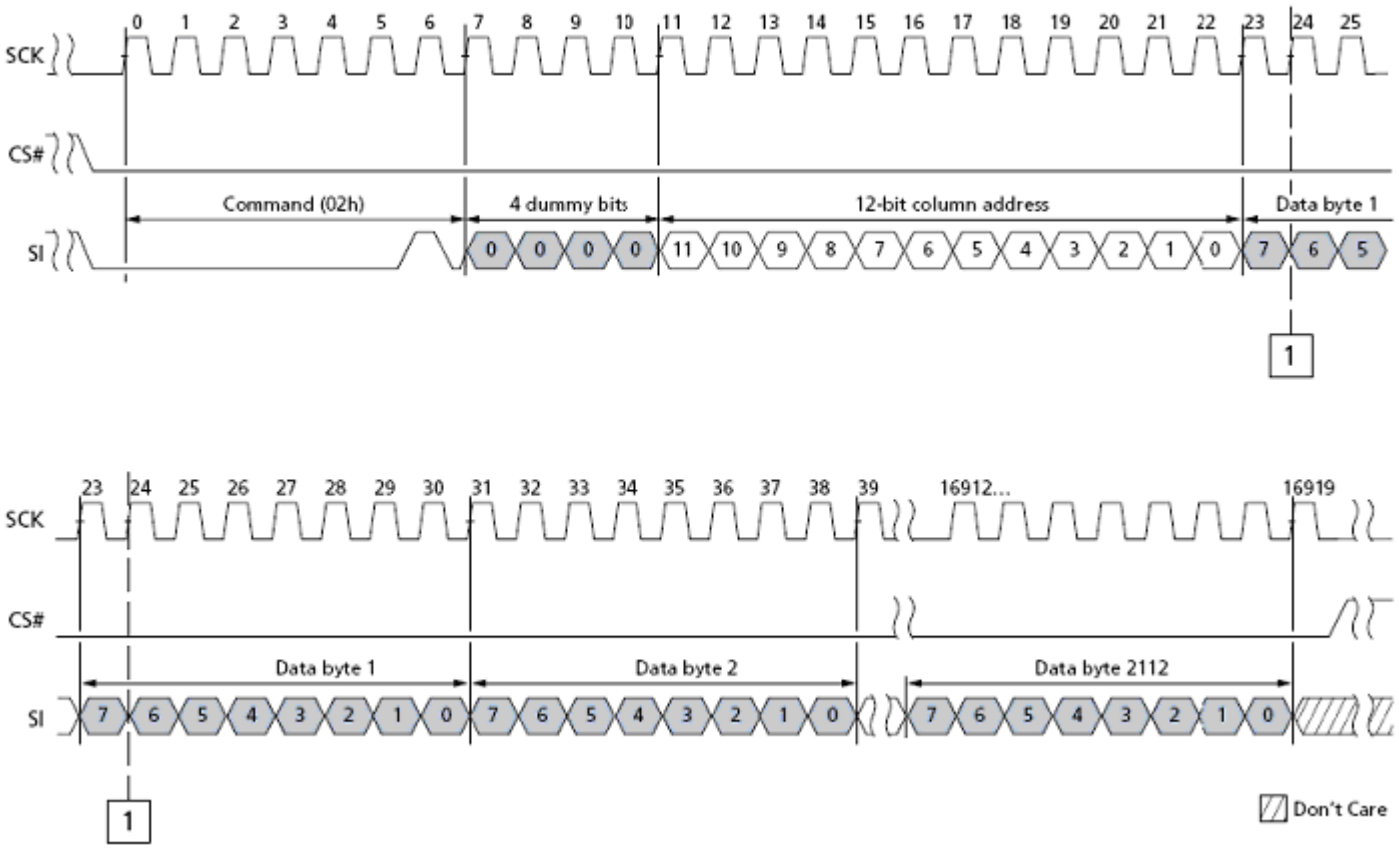
The command sequence is follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD x1) / 32h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

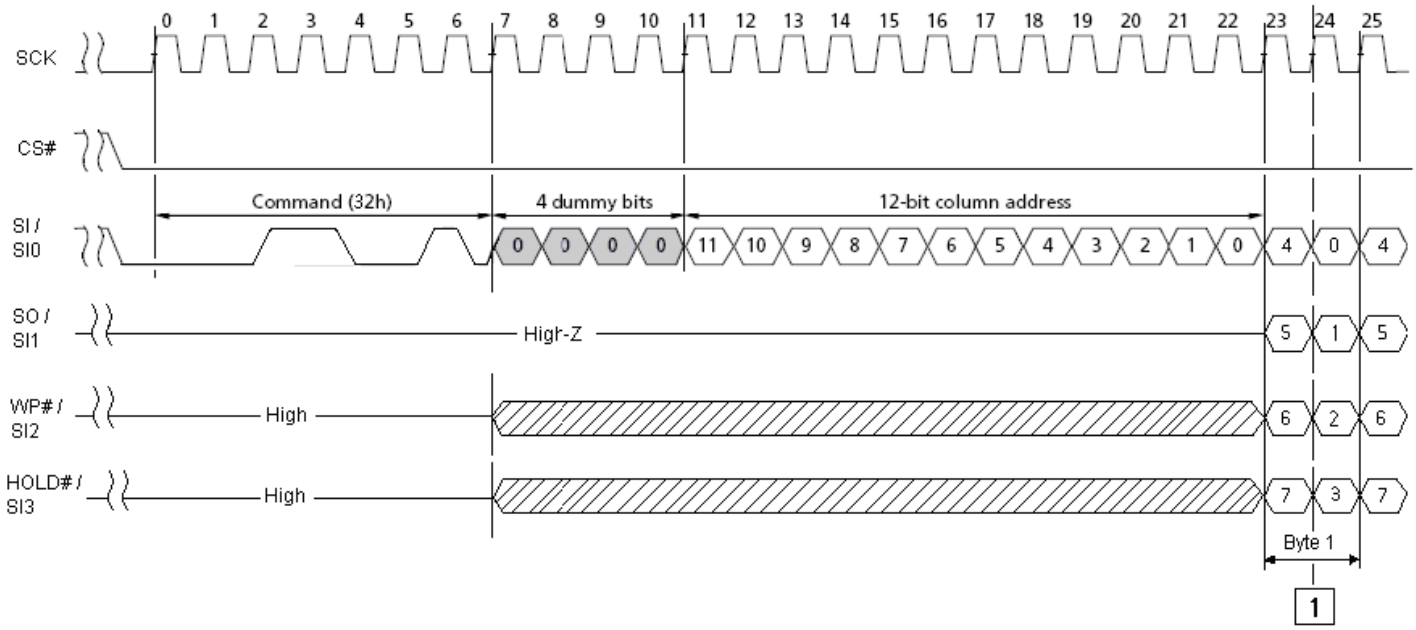
The page program operation sequence programs 1 byte to 2112 bytes of data within a page. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the program sequence is ignored. PROGRAM LOAD command requires 16-bit address with 4 dummy and a 12-bit column address, then the data bytes to be loaded into cache register. Only four partial page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register.

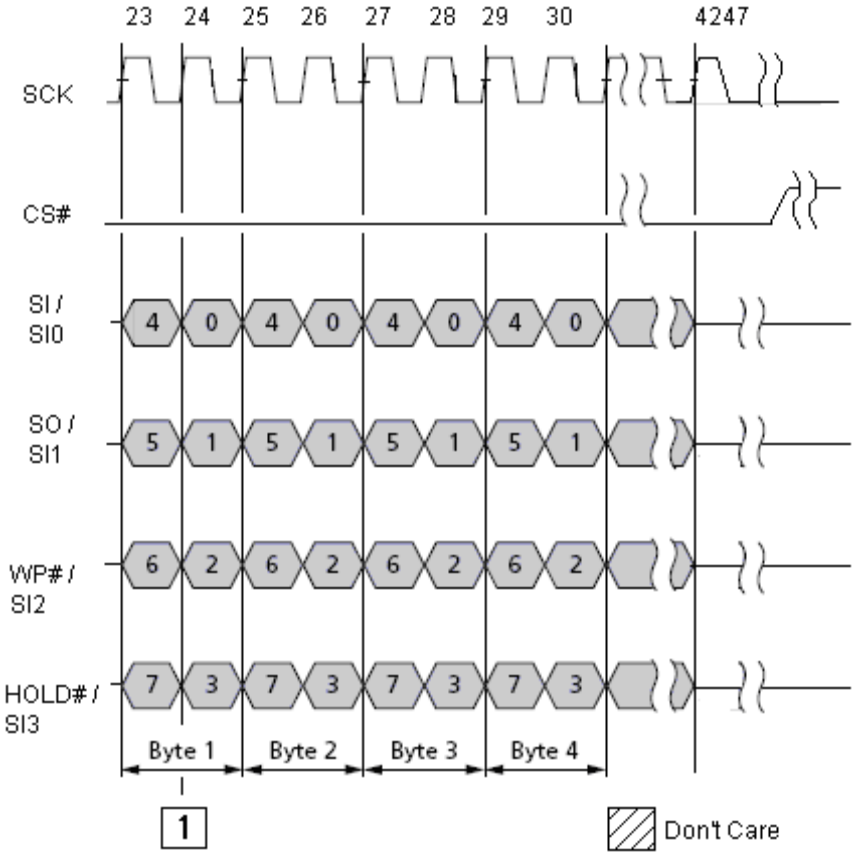
After the data is loaded, PROGRAM EXECUTE command must be issued to transfer the data from cache register to main array, and is busy for t_{PROG} time. PROGRAM EXECUTE command requires 24-bit address with 8 dummy bits and a 16-bit row address.

PROGRAM LOAD (02h) Timing

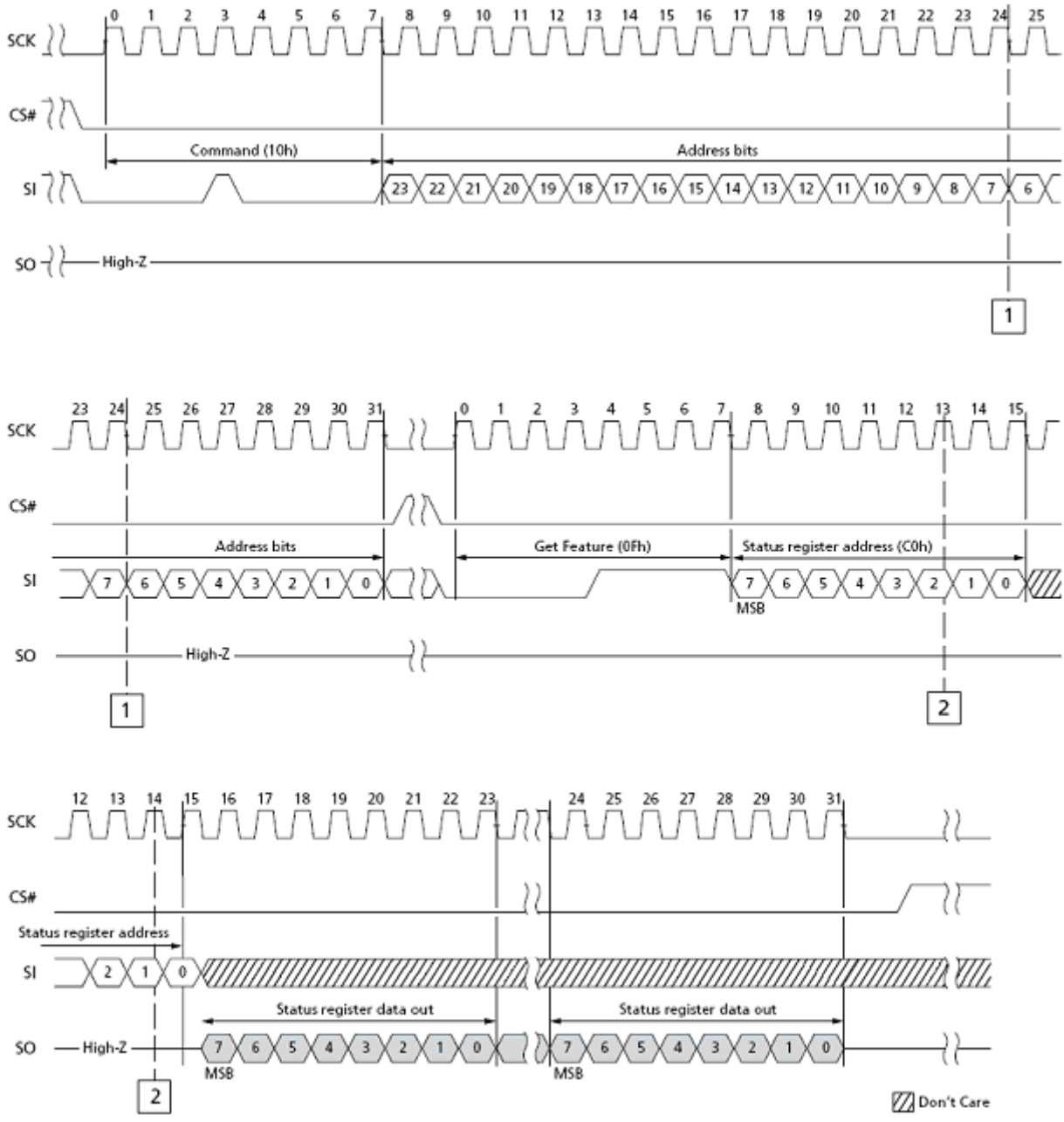


PROGRAM LOAD x4 (32h) Timing





PROGRAM EXECUTE (10h) Timing



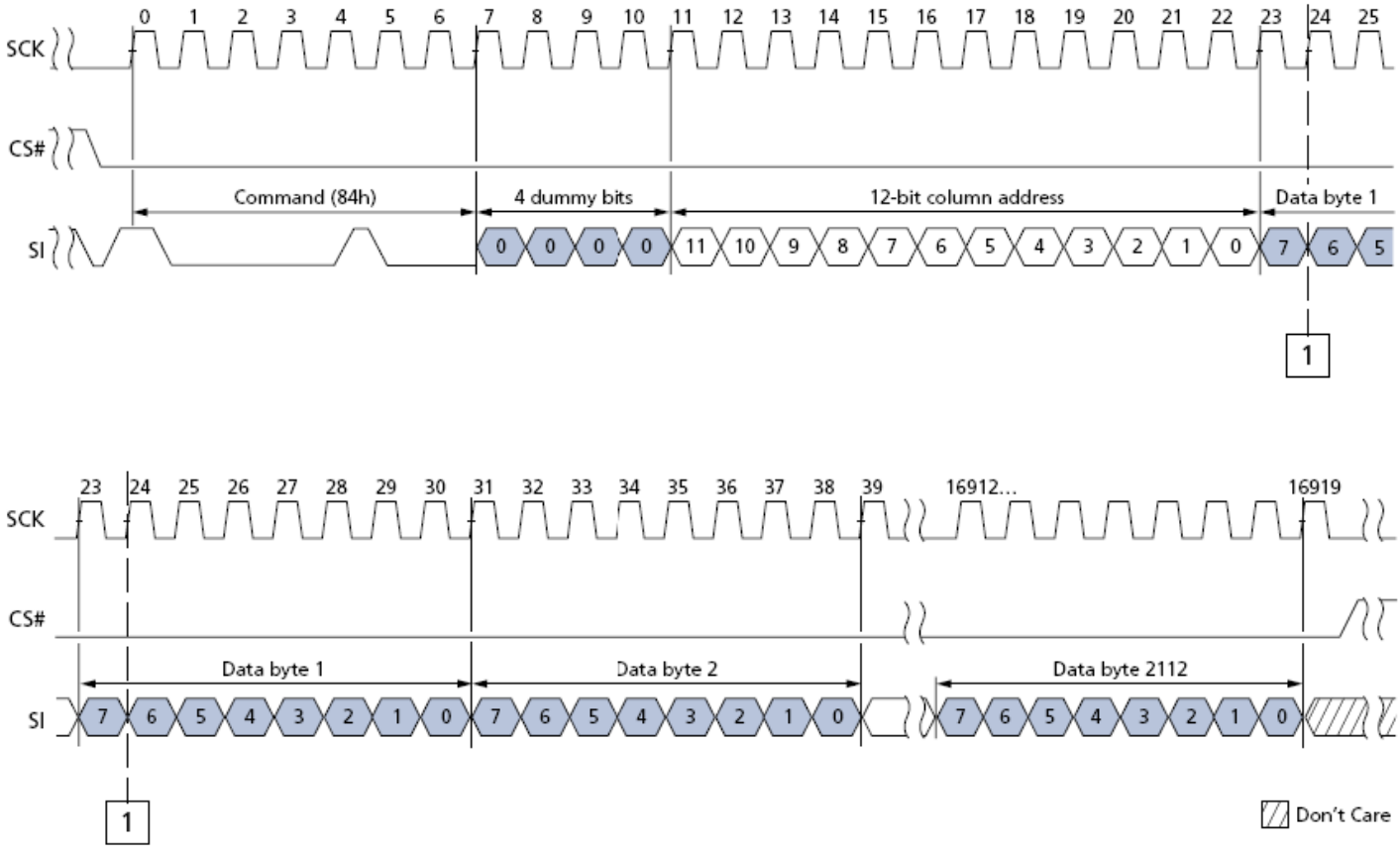
Random Data Program

The command sequence is follows:

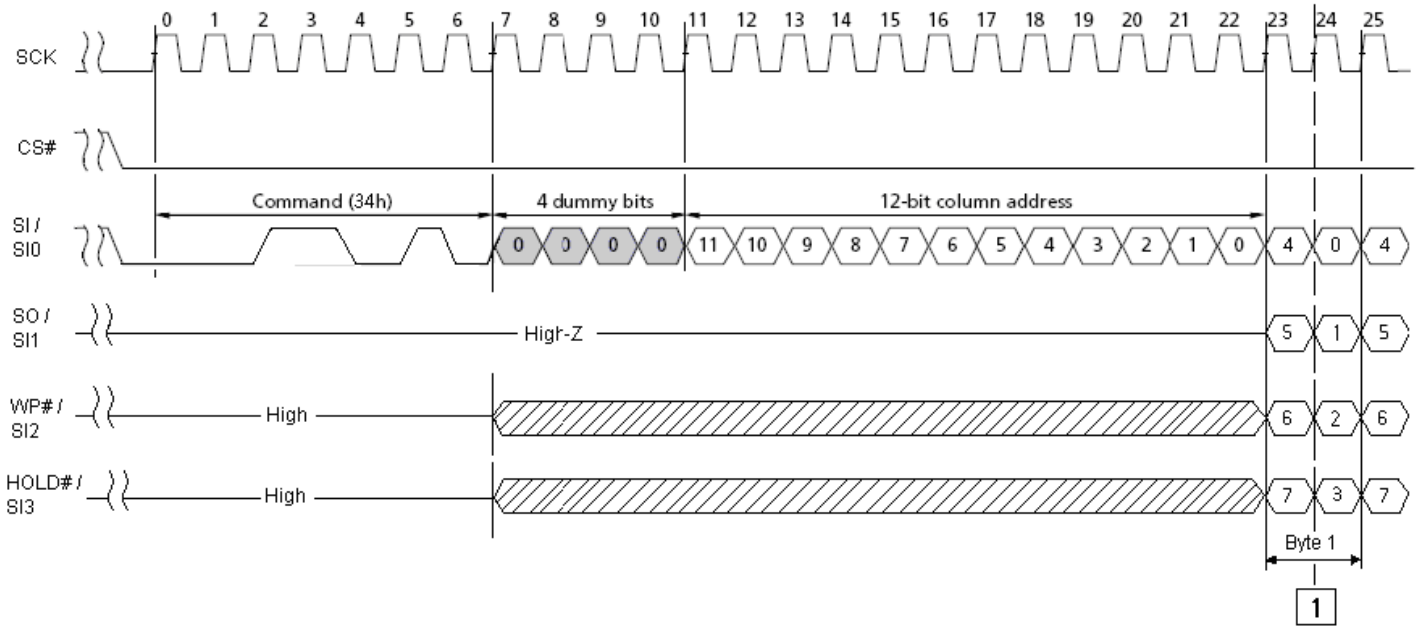
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

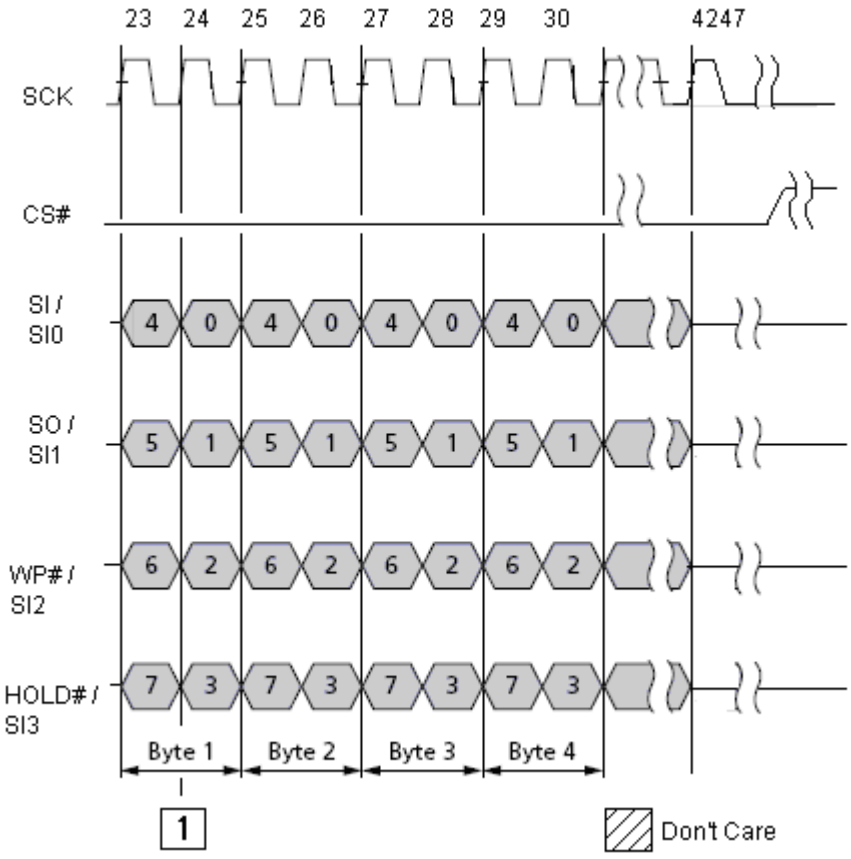
The random data program operation sequence programs or replaces data in a page with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.

PROGRAM LOAD RANDOM DATA (84h) Timing

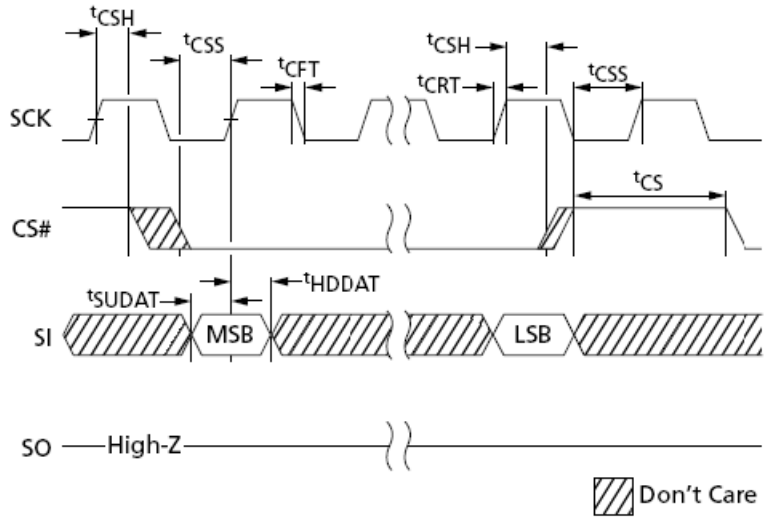


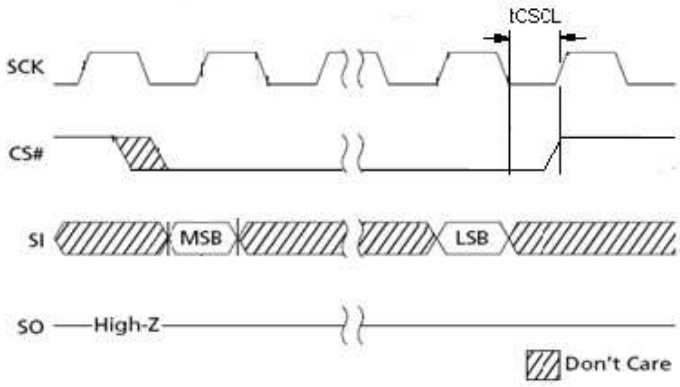
PROGRAM LOAD RANDOM DATA x4 (34h) Timing





Serial Input and t_{CSCL} Timing





Internal Data Move

The command sequence is follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4); this is OPTIONAL in sequence.
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The INTERNAL DATA MOVE operation sequence programs or replaces data in a page with existing data. Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. PAGE READ command must be followed with a WRITE ENABLE command to change the contents of memory array.

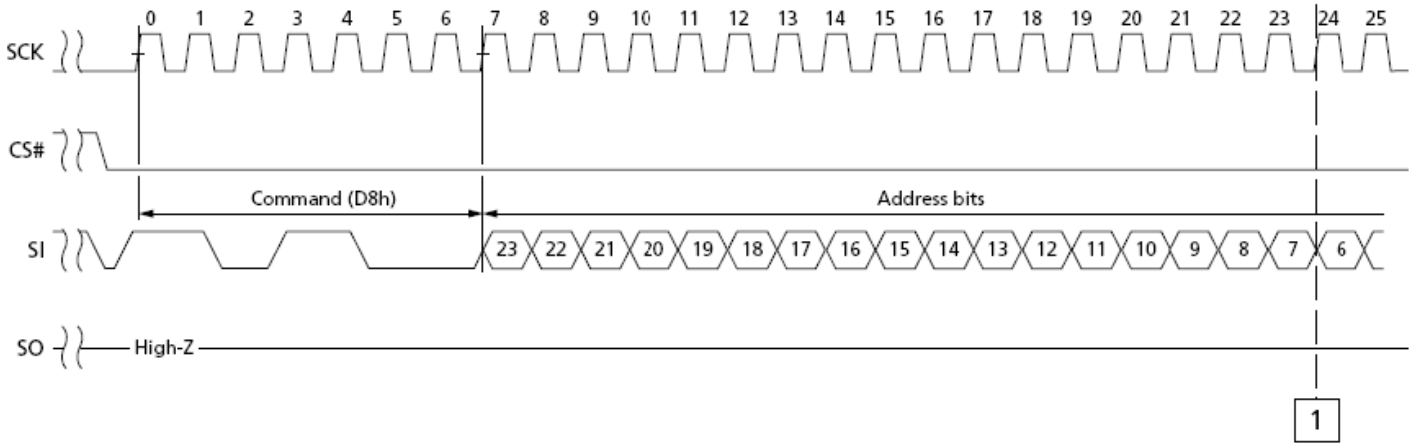
Erase Operation

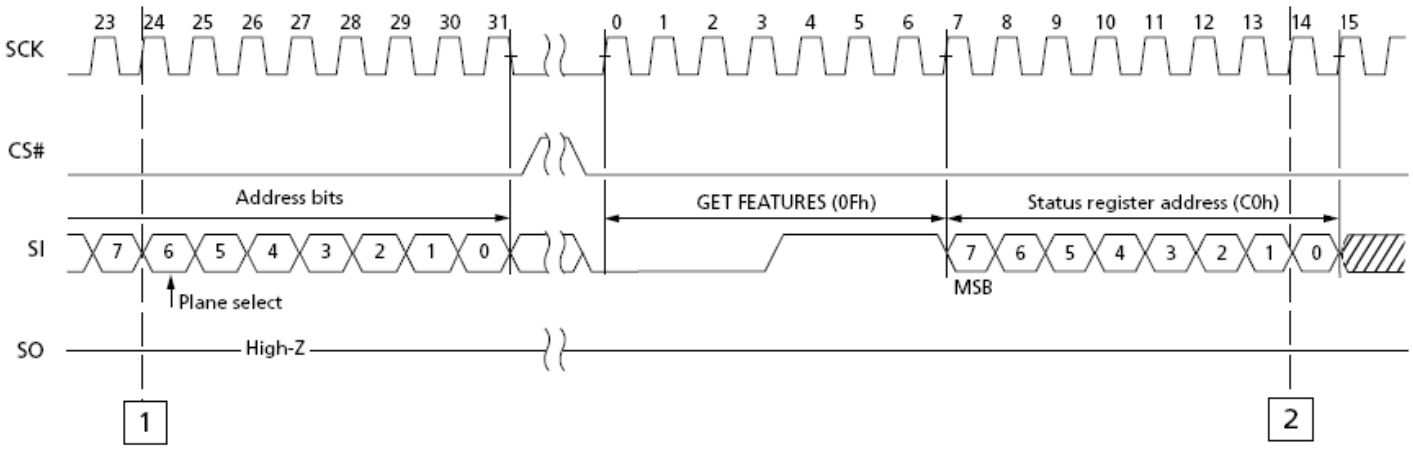
The command sequence is follows:

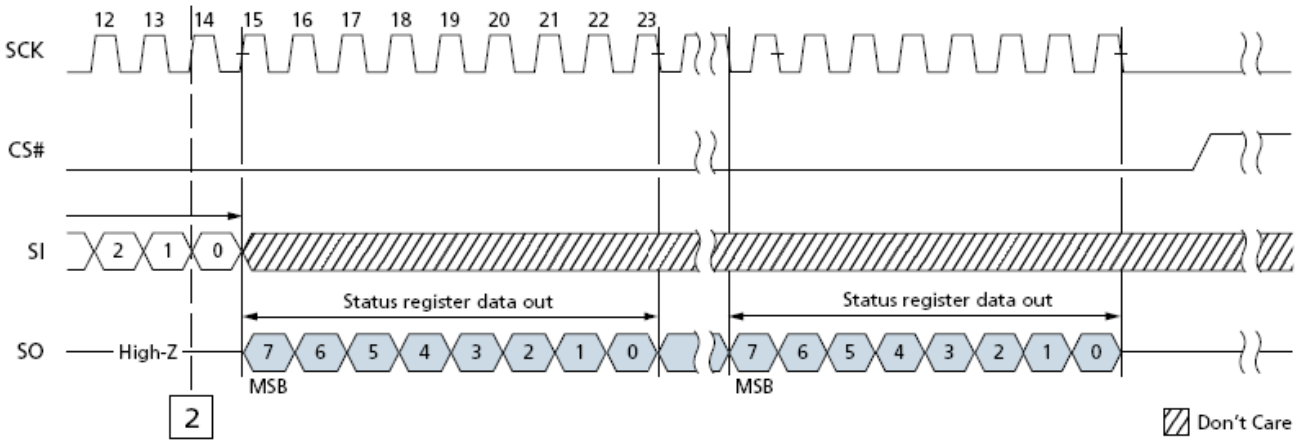
- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

BLOCK ERASE command requires 24-bit address with 8 dummy bits and a 16-bit row address. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the erase sequence is ignored. After the row address is registered, the control logic automatically controls the timing and the erase-verify operations, and the device is busy for t_{BERS} time. BLOCK ERASE command operates on one block at a time.

BLOCK ERASE (D8h) Timing



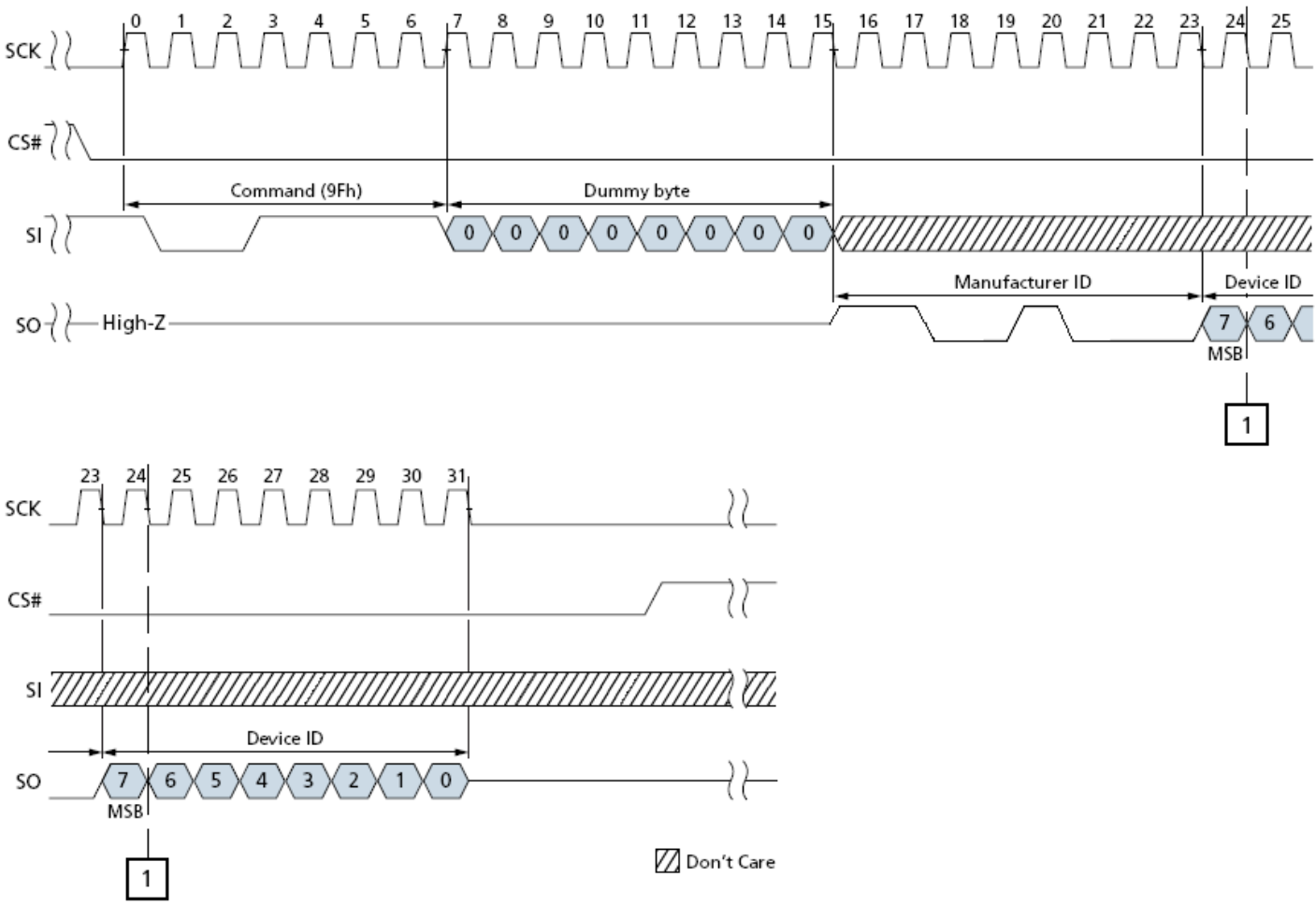




Read ID

The device contains a product identification mode, initiated by writing 9Fh to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5 th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

READ ID Timing

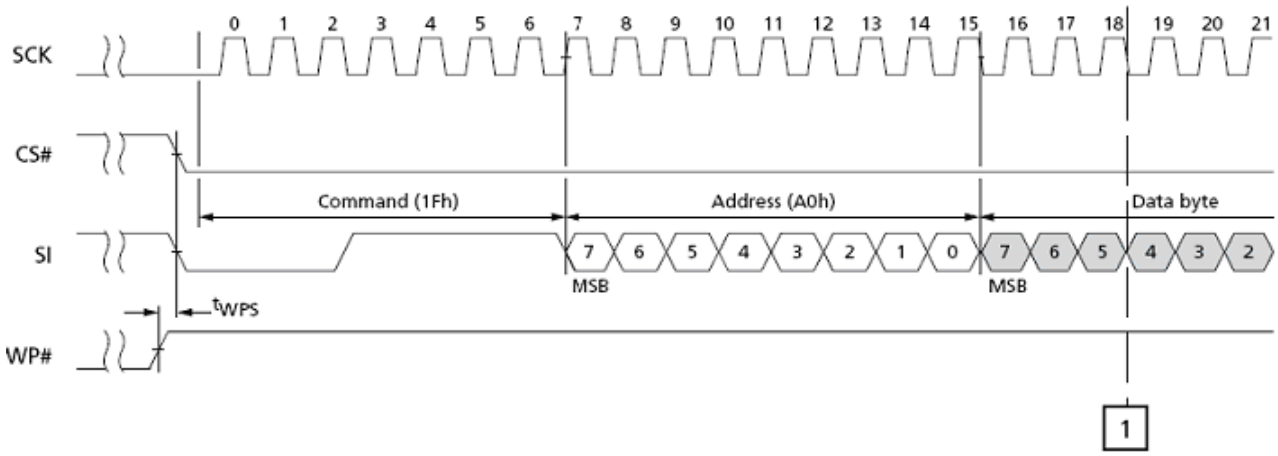


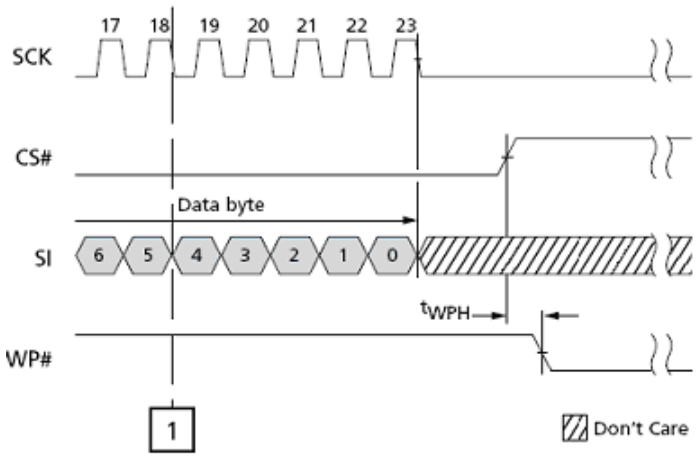
ID Definition Table

Product ID	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
F50L1G41A	C8h	21h	7Fh	7Fh	7Fh

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	JEDEC Maker Code Continuation Code, 7Fh
4th Byte	JEDEC Maker Code Continuation Code, 7Fh
5th Byte	JEDEC Maker Code Continuation Code, 7Fh

WP# Timing


SCK
CS#
SI
WP#
Command (1Fh)
Address (A0h)
Data byte
MSB
MSB
tWPS
1

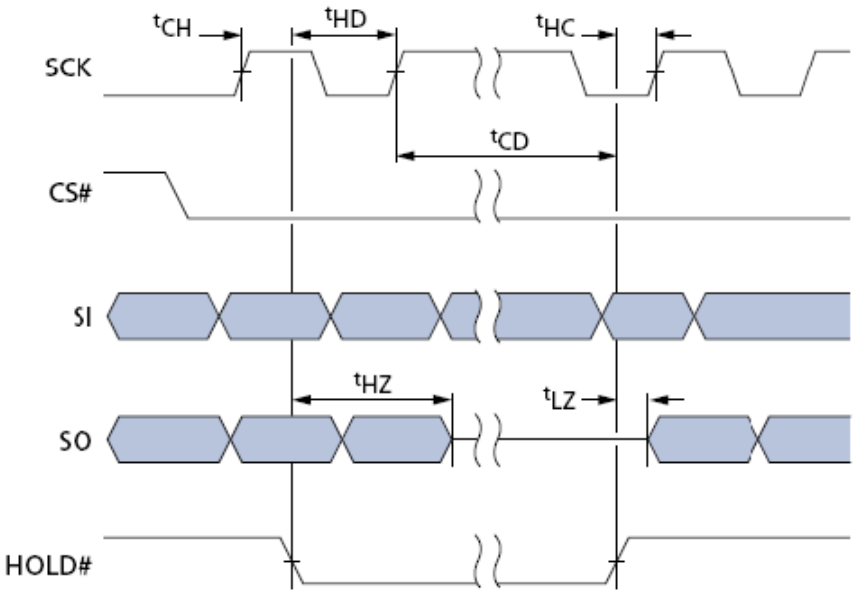

SCK
CS#
SI
WP#
Data byte
tWPH
1
Don't Care

HOLD# Timing

HOLD# input provides a method to pause serial communication with the device but doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.

Hold mode starts at the falling edge of HOLD# provided SCK is also Low. If SCK is High when HOLD# goes Low, hold mode begins after the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also Low. If SCK is High, hold mode ends after the next falling edge of SCK.

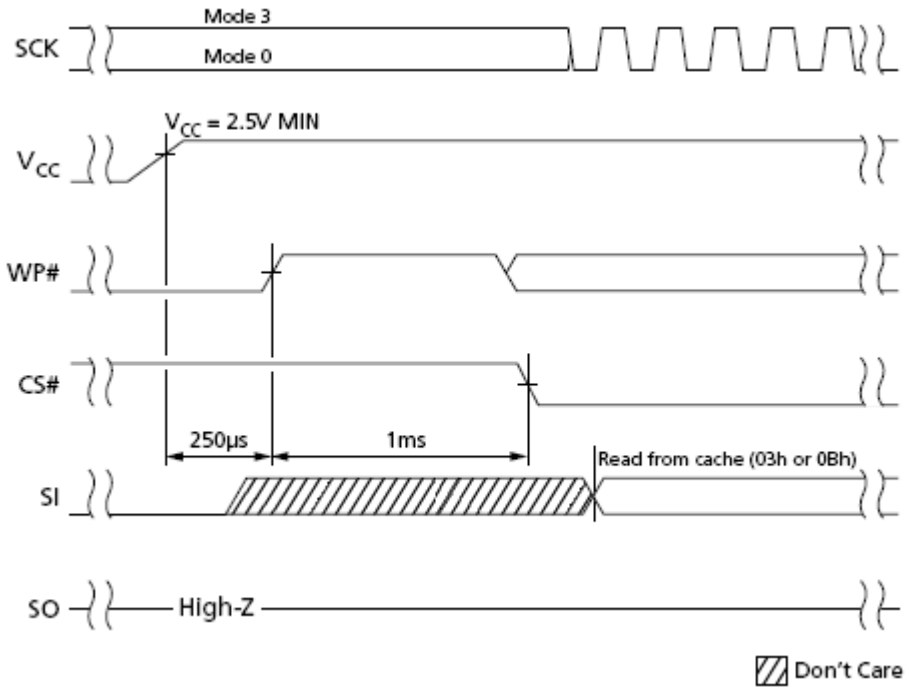
During hold mode, SO is Hi-Z, and SI and SCK inputs are ignored.



Power-Up

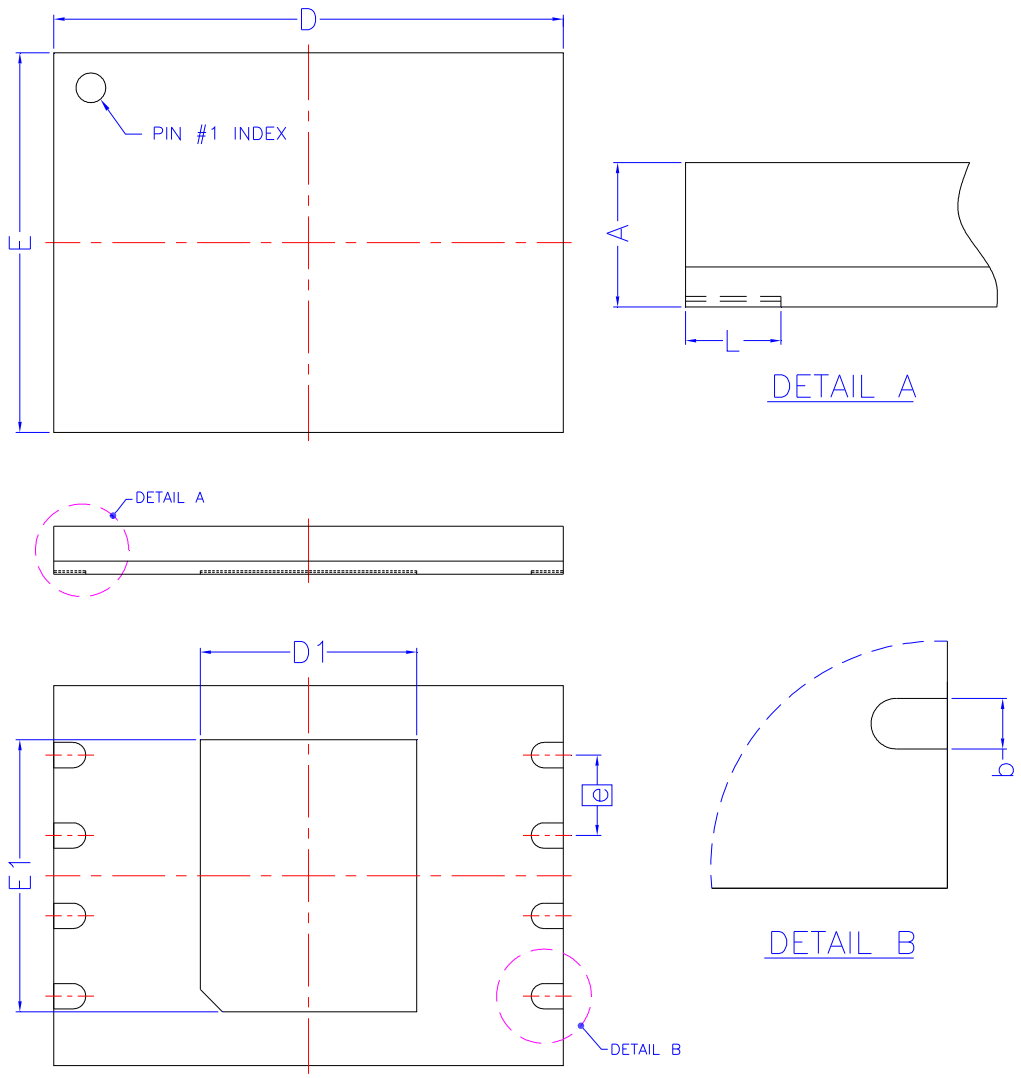
During power transitions, V_{CC} is internally monitored. 250us after V_{CC} has reached 2.5V, WP# is taken High, the device automatically performs the RESET command. The first access to the SPI NAND device can occur 1ms after WP# goes High, and then CS# can be driven Low, SCK can start, and the required command can be issued to the device.

Power-Up and RESET Timing



PACKING DIMENSIONS

8-Contact LGA (8x6 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
b	0.35	0.40	0.48	0.014	0.016	0.019
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	1.90	2.00	2.10	0.075	0.079	0.083
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		1.27 BSC			0.050 BSC	
L	0.40	0.50	0.60	0.016	0.020	0.024

Controlling dimension : millimeter

(Revision date : Feb 13 2014)

Revision History

Revision	Date	Description
0.1	2014.01.14	Original
0.2	2014.02.19	Add LGA package
1.0	2014.04.17	1. Delete "Preliminary" 2. Delete WSON package
1.1	2014.05.27	Modify the description of Identifying Initial Invalid Blocks
1.2	2014.08.15	Add the table of Array Address
1.3	2014.10..20	Modify D1 and E1 value in packing dimension
1.4	2015.07.01	Correct typo
1.5	2015.09.15	Modify ECC Protection Table
1.6	2016.07.22	Modify the specification of tHO
1.7	2018.01.02	Modify 8-Contact LGA (8x6 mm) PACKING DIMENSIONS

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express , implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.