DDR4 SDRAM

32M x 16 Bit x 8 Banks DDR4 SDRAM

Feature

- Power supply
  - VDD = VDDQ = 1.2V ± 5%
  - VPP = 2.375V to 2.75V
- 8 internal banks
  - 2 groups of 4 banks each (x16)
- Differential clock inputs (CK_t and CK_c)
- Bi-directional differential data strobe (DQS_t and DQS_c)
- Asynchronous reset is supported (RESET_n)
- ZQ calibration for Output driver by compare to external reference resistance (RZQ 240 ohm ±1%)
- Nominal, park and dynamic On-die Termination (ODT)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge
- CAS Latency (CL): 9, 11, 12, 13, 14, 15, 16, 18,19, 20, 21, 22, 23 and 24 supported
- Additive Latency (AL) 0, CL-1, and CL-2 supported
- Burst Length (BL): 8 and 4 with on the fly supported
- CAS Write Latency (CWL): 9, 10, 11, 12, 14, 16, 18 and 20 supported
- Refresh cycles
  Average refresh period
  - 7.8μs at 0°C ≤ T_C ≤ +85°C
  - 3.9μs at +85°C < T_C ≤ +95°C
- Fine granularity refresh is supported
- Adjustable internal generation VREFDQ
- Pseudo Open Drain (POD) interface for data input/output
- Driver strength selected by MRS
- The high-speed data transfer by the 8 bits prefetch
- Temperature Controlled Refresh (TCR) mode is supported
- Low Power Auto Self Refresh (LPASR) mode is supported
- Self-refresh abort is supported
- Programmable preamble is supported
- Write leveling is supported
- Command/Address latency (CAL) is supported
- Multipurpose register READ and WRITE capability
- Command Address (CA) Parity for command/address signal error detect and inform it to controller
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation
- Data Bus Inversion (DBI) for Improve the power consumption and signal integrity of the memory interface (x16 product only)
- Data Mask (DM) for write data
- Per DRAM Addressability (PDA) for each DRAM can be set a different mode register value individually and has individual adjustment.
- Gear down mode (1/2 and 1/4 rate) is supported
- PPR and sPPR is supported
- Connectivity test (x16 only)
- Maximum power down mode for the lowest power consumption with no internal refresh activity
- JEDEC JESD-79-4 compliant
- Operating case temperature range: T_C = 0°C to +95°C

Ordering Information

Product ID	Max Freq.	VDD	Data Rate (CL-tRCD-tRP)	Package	Comments
M16U4G16256A-QLBG	1600MHz	1.2V	DDR4- 3200 (24-24-24)	96 ball BGA	Pb-free
M16U4G16256A-KJBG	1333MHz	1.2V	DDR4- 2666 (19-19-19)	96 ball BGA	Pb-free
M16U4G16256A-HHBG	1200MHz	1.2V	DDR4- 2400 (17-17-17)	96 ball BGA	Pb-free

DDR4 SDRAM Addressing

Parameter	256 Mb x16
# of Bank	2
Bank group address	BG0
Bank count per group	4
Bank address in bank group	BA0 – BA1
Row addressing	A0 – A14
Column addressing	A0 – A9
Page size[1]	2KB

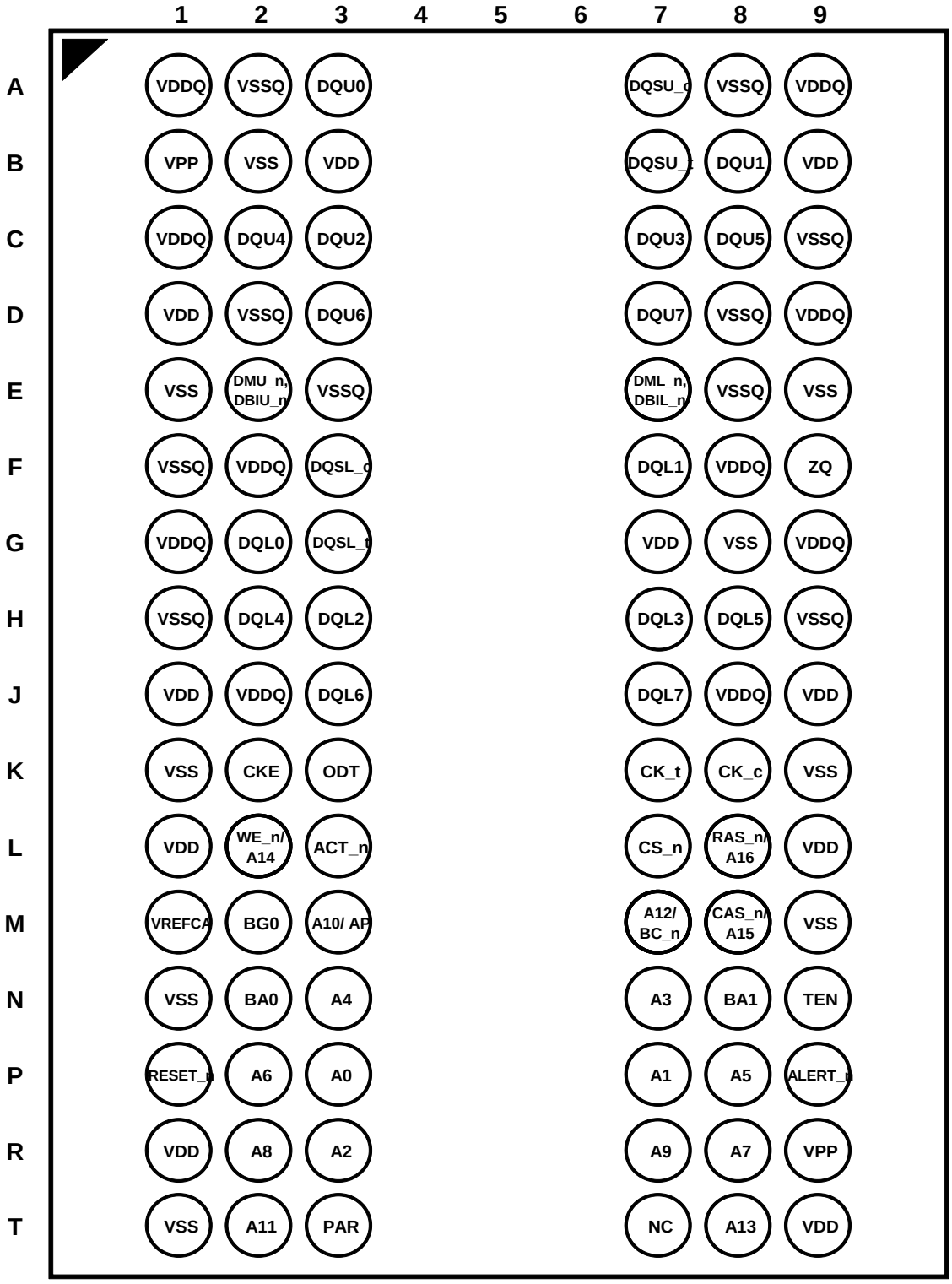
Note:

1. Page size is per bank, calculated as follows:
   Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

Ball Configuration – 96 balls BGA Package

< TOP View>

See the balls through the package



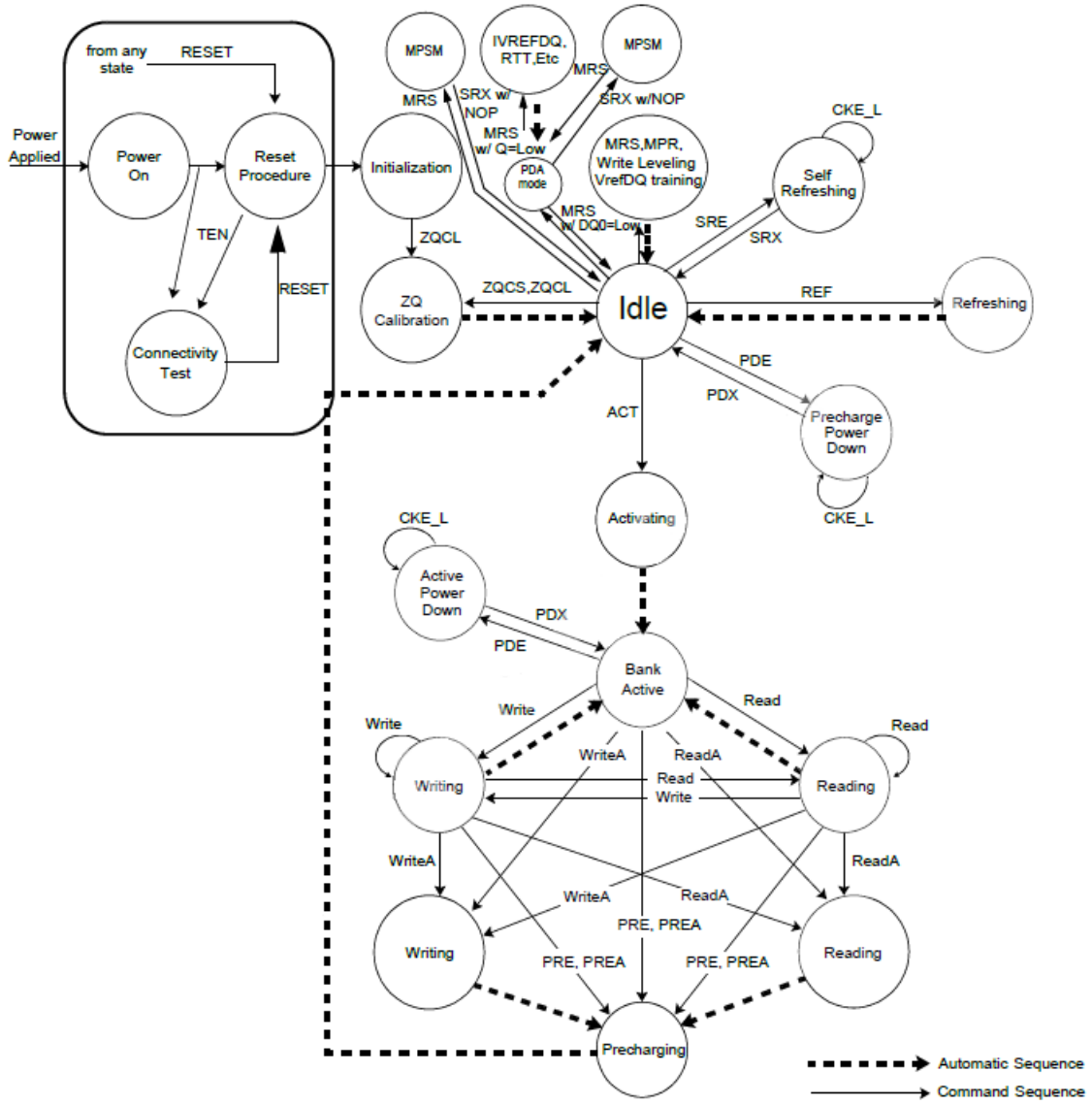
Input / Output Functional Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n, CAS_n/A15 and WE_n/A14 will be considered as Row Address A15 and A14
RAS_n, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A15, A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_nis sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.

Symbol	Type	Function
A0 - A15	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP,A12/ BC_n, RAS_n, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Setcommands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether thePrecharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity withACT_n,RAS_n,CAS_n/A15,WE_n/ A14,BG0-BG1,BA0-BA1,A15-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable : Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to V_{SS}.
NC		**No Connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.2 V +/- 0.06 V
VSSQ	Supply	**DQ Ground**

VDD	Supply	**Power Supply:** 1.2 V +/- 0.06 V
VSS	Supply	**Ground**
VPP	Supply	**DRAM Activating Power Supply:** 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference Pin for ZQ calibration**
Note: Input only pins (BG0-BG1, BA0-BA1, A0-A15, ACT_n, RAS_n, CAS_n/A15, W E_n/A14, CS_n, CKE, ODT, and RESET_n) do not supplytermination.		

Simplified State Diagram



State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET_n	Start RESET Procedure	MPR	Multi-Purpose Register
TEN	Boundary Scan Mode Enable	-	-	-	-

Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR settings need to be defined.

Gear down mode (MR3 A[3]) : 0 = 1/2 Rate
Per DRAM Addressability (MR3 A[4]) : 0 = Disable
Max Power Saving Mode (MR4 A[1]) : 0 = Disable
CS to Command/Address Latency (MR4 A[8:6]) : 000 = Disable
CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable
Hard Post Package Repair mode (MR4 A[13]) : 0 = Disable
Soft Post Package Repair mode (MR4 A[5]) : 0 = Disable

Power-up Initialization sequence

The Following sequence is required for POWER UP and Initialization

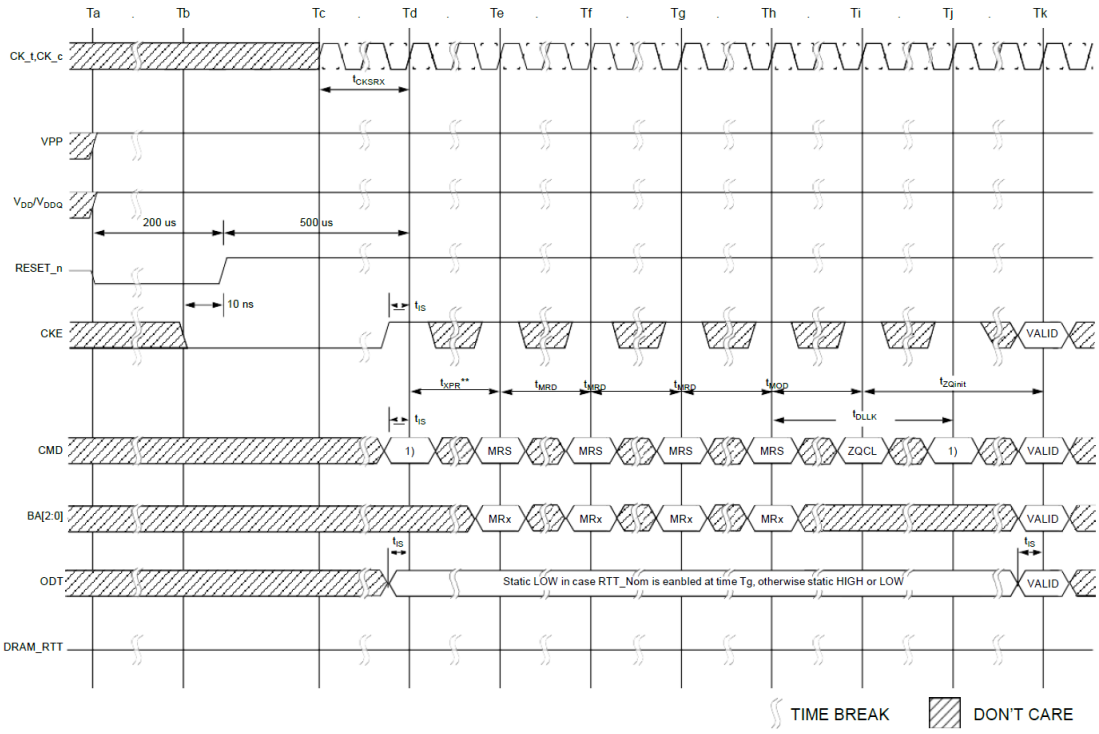
1. Apply power (RESET_n and TEN are recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). RESET_n needs to be maintained below 0.2 x VDD for minimum 200µs with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD_{min} must be no greater than 200ms; and during the ramp, VDD ≥ VDDQ and (VDD-VDDQ) <0.3 Volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.76 V max once power ramp is finished, AND
   - VrefCA tracks VDD/2.

OR

   - Apply VDD without any slope reversal before or at the same time as VDDQ
   - Apply VDDQ without any slope reversal before or at the same time as VTT & VrefCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After RESET_n is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clock (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a Deselect command must be registered (with tIS set up time to clock) at clock edge Td. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQ_{init}.
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as RESET_n is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET_n deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQ_{init}.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5nCK)]
6. Issue MRS Command to to load MR3 with all application settings(To issue MRS command to MR3, provide " Low" to BG0, "High" to BA1, BA0)
7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide "Low" to BA0, "High" to BG0, BA1)
8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide "Low" to BA1, "High" to BG0, BA0)
9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide "Low" to BA1, BA0, "High" to BG0)
10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide "Low" to BG0, BA0, "High" to BA1)
11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide "Low" to BG0, BA1, "High" to BA0).
12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide "Low" to BG0, BA1, BA0)
13. Issue ZQCL command to starting ZQ calibration
14. Wait for both tDLLK and tZQ init completed
15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).



RESET_n and Initialization Sequence at Power- on Ramping

Note:

1. From time point “Td” until “Tk”, DES commands must be applied between MRS and ZQCL commands.
2. MRS Commands must be issued to all Mode Registers that have defined settings.

VDD Slew rate at Power-up Initialization Sequence

VDD Slew Rate

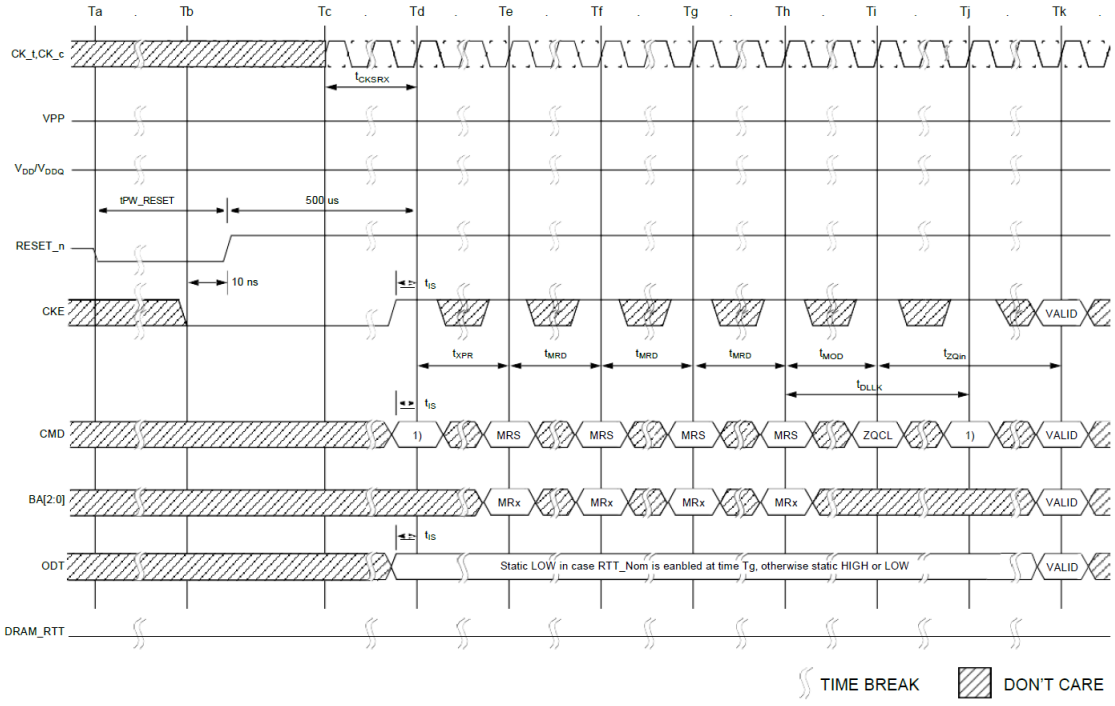
Symbol	Min	Max	Unit
VDD_sl[a]	0.004	600	V/ms[b]
VDD_ona		200	ms[c]

a. Measurement made between 300mv and 80% VDD minimum.
b. 20 MHz bandlimited measurement.
c. Maximum time to ramp VDD from 300 mv to VDD minimum.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET_n below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET_n needs to be maintained for minimum tPW_RESET. CKE is pulled "LOW" before RESET_n being de-asserted (min. time 10 ns).
2. Follow steps 2 to 10 in “Power-up Initialization Sequence”.
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include Vref training and Write leveling)



Reset Procedure at Power Stable

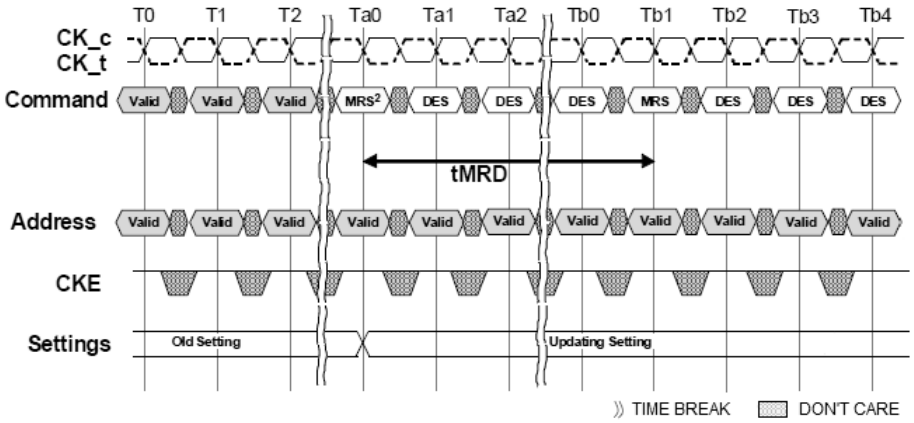
Note:

1. From time point ‘Td’ until ‘Tk’, DES commands must be applied between MRS and ZQCL commands
2. MRS Commands must be issued to all Mode Registers that have defined settings.

Register Definition

Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

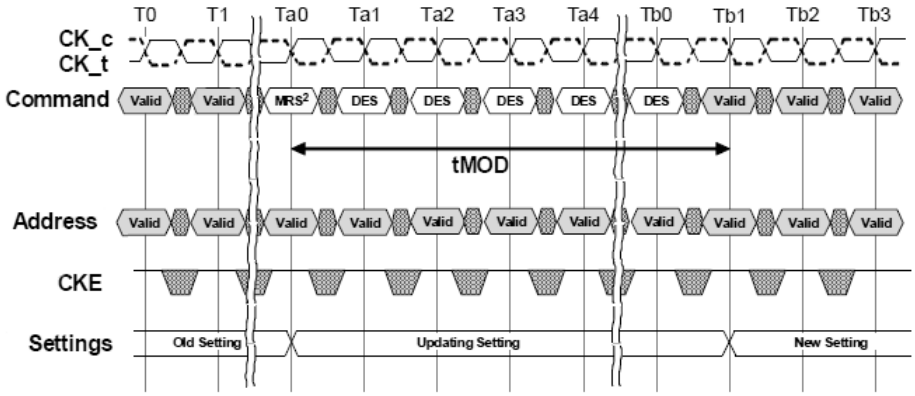


tMRD Timing

Note:

1. This timing diagram shows C/A Parity Latency mode is “Disable” case.
2. List of MRS commands exception that do not apply to tMRD
   - Gear down mode
   - C/A Parity Latency mode
   - CS to Command/Address Latency mode
   - Per DRAM Addressability mode
   - VrefDQ training Value, VrefDQ Training mode and VrefDQ training Range

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.
The MRS commands that do not apply tMRD timing to next MRS command are listed in Note 2 of tMRD Timing figure.
These MRS command input cases have unique MR setting procedure, so refer to individual function description.
The most MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES shown in tMOD Timing figure.

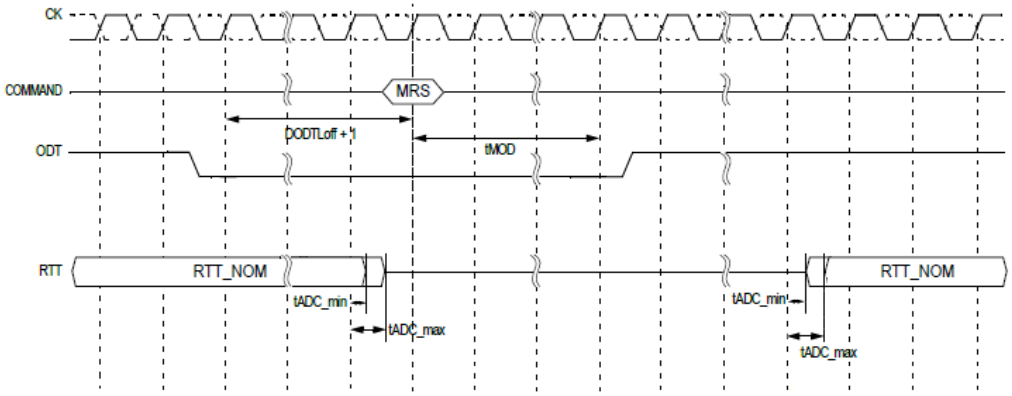


tMOD Timing

Note:

1. This timing diagram shows CA Parity Latency mode is “Disable” case.
2. List of MRS commands exception that do not apply to tMOD
   - DLL Enable, DLL Reset
   - VrefDQ training Value, internal Vref Monitor, VrefDQ Training mode and VrefDQ training Range
   - Gear down mode
   - Per DRAM addressability mode
   - Maximum power saving mode
   - CA Parity mode

Some of the mode register setting cases, function updating takes longer than tMOD. The MRS commands that do not apply tMOD timing to next valid command excluding DES is listed in Note 2 of tMOD Timing figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



ODT Status at MRS affecting ODT turn-on/off timing

Note:

1. This timing diagram shows CA Parity Latency mode is “Disable” case.
2. When an MRS command mentioned in this note affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value, this means the MR register value changes. The ODT signal should set to be low for at least DODTLoff +1 clock before their affecting MRS command is issued and remain low until tMOD expires. The following MR registers affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value and it requires ODT to be low when an MRS command change the MR register value. If there are no change the MR register value that correspond to commands mentioned in this note, then ODT signal is not require to be low.
   - DLL control for precharge power down
   - Additive latency and CAS read latency
   - DLL enable and disable
   - CAS write latency
   - CA Parity mode
   - Gear Down mode
   - RTT_NOM

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of ODT Status at MRS affecting ODT turn-on/off timing figure for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don’t care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.

Mode Register

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13[5], A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge (see Write Recovery and Read to Precharge (cycles) table)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A12, A6:A4,A2	CAS Latency[4]	(see CAS Latency table)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) Abbreviated BL8MRS 01 = BC4 or 8 (on the fly) Abbreviated BC4OTF or BL8OTF 10 = BC4 (Fixed) Abbreviated BC4MRS 11 = Reserved

Note:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated following rounding algorithm defined.
   The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency. Cas Latency controlled by A12 is optional for 4Gb device.
5. A13 for WR and RTP setting is optional for 4Gb.

Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	22	11
0	1	1	1	24	12
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27 (only 3DS available)
1	0	0	1	1	28
1	0	1	0	0	reserved for 29
1	0	1	0	1	30
1	0	1	1	0	reserved for 31
1	0	1	1	1	32
1	1	0	0	0	reserved

Mode Register 1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[3]
A17	RFU	0 = must be programmed to 0 during MRS
A13, A6, A5	Rx CTLE control	000 = Vendor Optimized Setting (default) 001 = vendor defined 010 = vendor defined 011 = vendor defined 100 = vendor defined 101 = vendor defined 110 = vendor defined 111 = vendor defined
A12	Qoff[1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see RTT_NOM table)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A4, A3	Additive Latency	00 = 0(AL disabled) 10 = CL-2 01 = CL-1 11 = Reserved
A2, A1	Output Driver Impedance Control	(see Output Driver Impedance Control table)
A0	DLL Enable	0 = Disable[2] 1 = Enable

Note:

1. Outputs disabled - DQs, DQS_ts, DQS_cs.
2. States reversed to “0 as Disable” with respect to DDR4.
3. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

Mode Register 2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
A11, A10:A9	RTT_WR	(see RTT_WR table)
A8, A2	RFU	0 = must be programmed to 0 during MRS
A7:A6	Low Power Auto Self Refresh (LP ASR)	00 = Manual Mode (Normal Operaing Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency(CWL)	see CWL (CAS Write Latency) table)
A1:A0	RFU	0 = must be programmed to 0 during MRS

Note:

1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CWL (CAS Write Latency)

A5	A4	A3	CWL	Operating Data Rate in MT/s for 1 tCK Write Preamble		Operating Data Rate in MT/s for 2 tCK Write Preamble[1]	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	2933/ 3200	2400	2666	2400
1	1	0	18		2666	2933 / 3200	2666
1	1	1	20		2933 / 3200		2933 / 3200

Note:

1. The 2 tCK Write Preamble is valid for DDR4-2400/2666/2933/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

Mode Register 3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A11	MPR Read Format	00 = Serial 10 = Staggered 01 = Parallel 11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	see Write Command Latency when CRC and DM are both enabled table
A8, A6	Fine Granularity Refresh Mode	see Fine Granularity Refresh Mode table
A5	Temperature sensor readout	0 = Disable 1 = Enable
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 10 = Page2 01 = Page 1 11 = Page3 (see MPR Data Format table)

Note:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write Command Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866,2133,2400,2666
1	0	6nCK	2933,3200
1	1	RFU	RFU

Note:

1. Write Command latency when CRC and DM are both enabled:
2. At less than or equal to 1600 then 4nCK; neither 5nCK nor 6nCK
3. At greater than 1600 and less than or equal to 2666 then 5nCK; neither 4nCK nor 6nCK
4. At greater than 2666 and less than or equal to 3200 then 6nCK; neither 4nCK nor 5nCK

MPR page0 (Training Pattern)

MPR Data Format

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/ Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read only
	01 = MPR1	CAS_n/ A15	WE_n/ A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/ A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[4]			C[2]	C[1]	C[0]	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

Note:

1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.
4. MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status		CRC Write Enable	Rtt_WR		Read only
		—	—	MR2	—	—	MR2	MR2		
		—	—	A11	—	—	A12	A10	A9	
	01 = MPR1	Vref DQ Trng range	Vref DQ Trng range						Geardwn Enable	
		MR6	MR6						MR3	
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency					CAS Write Latency			
		MR0					MR2			
		A6	A5	A4	A2	A12	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance		
		MR1			MR5			MR1		
		A10	A9	A6	A8	A7	A6	A2	A1	

MR bit for Temperature Sensor Readout

MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> tREFI)
0	1	1X refresh rate(= tREFI)
1	0	2X refresh rate(1/2* tREFI)
1	1	rsvd

MPR page3 (Vendor use only)[1]

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	don't care								Read only
	01 = MPR1	don't care								
	10 = MPR2	don't care								
	11 = MPR3	don't care				MAC				

Note:

1. MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

Mode Register 4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	hPPR	0 = Disable 1 = Enable
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self Refresh Abort	0 = Disable 1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 001 = 3 010 = 4 011 = 5 100 = 6 101 = 8 110 = Reserved 111 = Reserved (see CS to CMD / ADDR Latency Mode Setting table)
A5	sPPR	0 = Disable 1 = Enable
A4	Internal Vref Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

Note:

1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

Mode Register 5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent	0 = Disable 1 = Enable
A8:A6	RTT_PARK	see RTT_PARK table
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	C/A Parity Latency Mode	see the table of C/A Parity Latency Mode table

Note:

1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	–
0	0	1	4	1600,1866,2133
0	1	0	5	2400, 2666
0	1	1	6	2933, 3200
1	0	0	8	RFU
1	0	1	Reserved	–
1	1	0	Reserved	–
1	1	1	Reserved	–

Note:

1. Parity latency must be programmed according to timing parameters by speed grade table

MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13, A9, A8	RFU	0 = must be programmed to 0 during MRS
A12:A10	tCCD_L	(see the table of "tCCD_L and tDLLK")
A7	VrefDQ Training Enable	0 = Disable (Normal operation Mode) 1 = Enable (Training Mode)
A6	VrefDQ Training Range	(see the table of "VrefDQ Training: Range")
A5:A0	VrefDQ Training Value	(see the table of "VrefDQ Training: Values")

Note:
1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1;BA0=111 and doesn't respond.

tCCD_L and tDLLK

A12	A11	A10	tCCD_L.min (nCK)[1]	tDLLKmin (nCK)[1]	Note
0	0	0	4	597	Data rate≦1333Mbps
0	0	1	5		1333Mbps < Data rate≦1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate≦2400Mbps (2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate≦2666Mbps (2666Mbps)
1	0	0	8		2666Mbps < Data rate≦3200Mbps (2933/3200Mbps)
1	0	1	Reserved	–	–
1	1	0			–
1	1	1			–

Note:
1. tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency

VrefDQ Training: Range

A6	VrefDQ Range
0	Range 1
1	Range 2

A5:A0	Range1	Range2	A5:A0	Range1	Range2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 111111	Reserved	Reserved

MR7 DRAM: Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM.Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power supply voltage	VDD	-0.3 to +1.5	V	1, 3
Power supply voltage for output	VDDQ	-0.3 to +1.5	V	1, 3
DRAM activation power supply	VPP	-0.3 to +3.0	V	4
Input voltage	VIN	-0.3 to +1.5	V	1
Output voltage	VOUT	-0.3 to +1.5	V	1
Reference voltage	VREFCA	-0.3 to 0.6 x VDD	V	3
Storage temperature	Tstg	-55 to +100	°C	1, 2

Notes:

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be no greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Temperature Range

Symbol	Parameter	Value	Units	Notes
T_C	Normal Operating Temperature Range	0 to 85	°C	1
	Extended Temperature Range	85 to 95	°C	1,2

Note:

1. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering.
2. Some applications require operation of the commercial and industrial temperature DRAMs in the extended temperature range (between 85°C and 95°C case temperature). Full specifications are supported in this range, but the following additional conditions apply:
   a) REFRESH commands must be doubled in frequency, reducing the refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the extended temperature range.
   b) If SELF REFRESH operation is required in the extended temperature range, it is mandatory to use either the manual self refresh mode with extended temperature range capability (MR2[6] = 0 and MR2 [7] = 1) or enable the optional auto self refresh mode (MR2 [6] = 1 and MR2 [7] = 1).

Operating Temperature Condition

Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	VDD	1.14	1.2	1.26	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.14	1.2	1.26	V	1, 2, 3
DRAM activating power	VPP	2.375	2.5	2.75	V	3
Ground	VSS	0	0	0	V	
Ground for DQ	VSSQ	0	0	0	V	

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

IDD and IDDQ Specification Parameters and Test conditions

IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined.
The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD, IPP and IDDQ measurements.

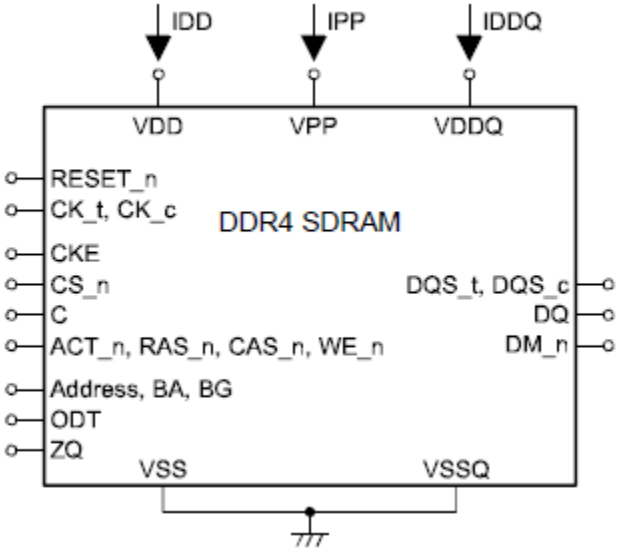
- IDD currents (such as IDD0, IDD0A, IDD1, IDD2N, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6N, IDD6E, IDD6A and IDD7) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Note: IDDQ values cannot be directly used to calculate I/O power of the DDR4 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD, IPP and IDDQ measurements, the following definitions apply:

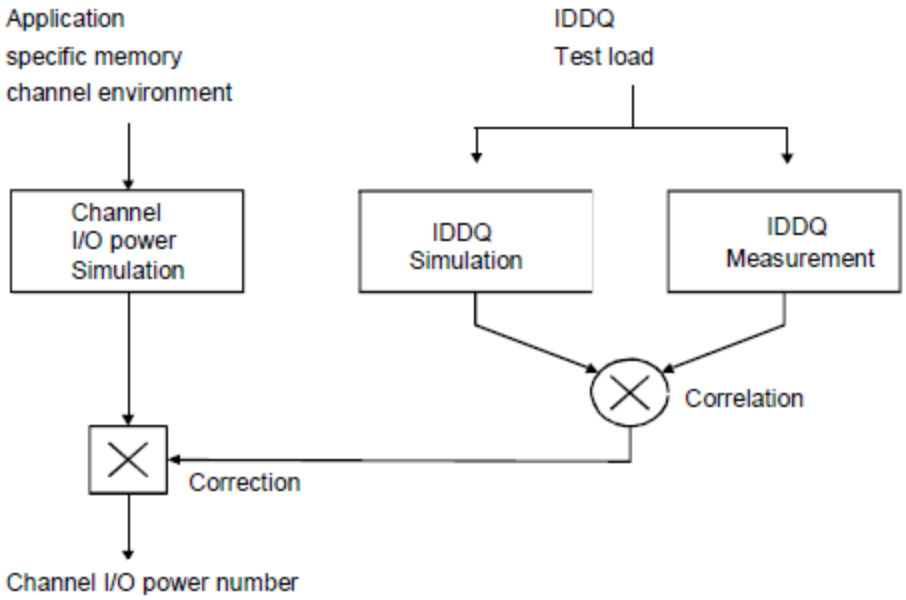
- L and 0: VIN ≤ VIL(AC) max
- H and 1: VIN ≥ VIH(AC) min
- MID-LEVEL: defined as inputs are VREFCA = VDD / 2
- Timings used for IDD, IPP and IDDQ measurement-loop patterns are provided in Timings Used for IDD and IDDQ Measurement-Loop Patterns table.
- Basic IDD, IPP and IDDQ measurement conditions are described in Basic IDD, IPP and IDDQ Measurement Conditions table.
  Note: The IDD, IPP and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Detailed IDD, IPP and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting.

  RON = RZQ/7 (34Ω in MR1);
  Qoff = 0B (Output buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40Ω in MR1);
  RTT_WR = RZQ/2 (120Ω in MR2);
  RTT_PARK = Disable;
  TDQS_t feature disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear-down mode disabled in MR3;
  Read/Write DBI disabled in MR5;
  DM_n disabled in MR5

- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, L, L, L, L} ; apply BG/BA changes when directed.
- Define /D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, H, H, H, H}; apply BG/BA changes when directed.



Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements



Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

Timings Used for IDD and IDDQ Measurement-Loop Patterns

Symbol	DDR4-2400 (17-17-17)	DDR4-2666 (19-19-19)	DDR4-3200 (24-24-24)	Unit
tCK	0.833	0.750	0.625	ns
CL	17	19	24	nCK
CWL	16	18	20	nCK
nRCD	17	19	24	nCK
nRC	56	62	76	nCK
nRAS	39	43	52	nCK
nRP	17	19	24	nCK
nFAW	36	40	48	nCK
nRRDS	7	7	9	nCK
nRRDL	8	9	11	nCK
tCCD_S	4	4	4	nCK
tCCD_L	6	7	8	nCK
tWTR_S	3	4	4	nCK
tWTR_L	9	10	12	nCK
nRFC 4Gb	313	347	416	nCK

Basic IDD and IDDQ Measurement Conditions

Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: H between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Measurement-Loop Pattern table); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Measurement-Loop Pattern table
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** AL = CL-1, Other conditions: see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** Same condition with IDD0
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: H between ACT, RD and PRE; Command, address, bank group address, bank address inputs, data I/O: partially toggling according to Measurement-Loop Pattern table; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Measurement-Loop Pattern table); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Measurement-Loop Pattern table
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** AL=CL-1, Other conditions : see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPPCurrent** Same condition with IDD1
IDD2N	**Precharge Standby Current (AL=0)** CKE: H; External clock: on; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Measurement-Loop Pattern table; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Measurement-Loop Pattern table
IDD2NA	**Precharge Standby Current (AL=CL-1)** Same condition with IDD2N
IPP2N	**Precharge Standby IPP Current** AL = CL-1, Other conditions: see IDD2N
IDD2NT	**Precharge Standby ODT Curren**t CKE: H; External clock: on; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Measurement-Loop Pattern table; data I/O: VSSQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to Measurement-Loop Pattern table
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled*3
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled*3,*5
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled*3
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled*3

IDD2P	**Precharge Power-Down Current** CKE: Low; External clock: on; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
IPP2P	**Precharge Power-Down IPP Current** Same condition with IDD2P
IDD2Q	**Precharge Quiet Standby Current** CKE: H; External clock: On; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
IDD3N	**Active Standby Current** CKE: H; External clock: on; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Measurement-Loop Pattern table; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Measurement-Loop Pattern table
IDD3NA	**Active Standby Current (AL=CL-1)** Same condition with IDD3N
IPP3N	**Active Standby IPP Current** AL = CL-1, Other conditions: see IDD3N
IDD3P	**Active Power-Down Current** CKE: L; External clock: on; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ; DM_n:stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
IPP3P	**Active Power-Down IPP Current** Same condition with IDD3P
IDD4R	**Operating Burst Read Current** CKE: H; External clock: on; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: H between RD; Command, address, Bank group address, Bank address Inputs: partially toggling according to Measurement-Loop Pattern table; data I/O: seamless read data burst with different data between one burst and the next one according to Measurement-Loop Pattern table; DM_n: stable at 1;Bank activity: all Banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Measurement-Loop Pattern table); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Measurement-Loop Pattern table
IDD4RA	**Operating Burst Read Current (AL=CL-1)** AL = CL-1, Other conditions: see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** Read DBI enabled*3, Other conditions: see IDD4R
IPP4R	**Operating Burst Read IPP Current** Same condition with IDD4R
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** CKE: H; External clock: on; tCK, CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: H between WR; command, address, bank group address, bank address inputs: partially toggling according to Measurement-Loop Pattern table; data I/O: seamless write data burst with different data between one burst and the next one according to Measurement-Loop Pattern table;DM_n: stable at 1; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,.. (see Measurement-Loop Pattern table); output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see Measurement-Loop Pattern table
IDD4WA	**Operating Burst Write Current (AL=CL-1)** AL = CL-1, Other conditions: see IDD4W

IDD4WB	**Operating Burst Write Current with Write DBI** Write DBI enabled*3, Other conditions: see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** Write CRC enabled*3, Other conditions: see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** CA Parity enabled*3, Other conditions: see IDD4W
IPP4W	**Operating Burst Write IPP Current** Same condition with IDD4W
IDD5B	**Burst Refresh Current (1X REF)** CKE: H; External clock: on; tCK, CL, nRFC: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n: H between REF; Command, address, bank group address, bank address Inputs: partially toggling according to Measurement-Loop Pattern table; data I/O: VDDQ; DM_n: stable at 1; bank activity: REF command every nRFC (Measurement-Loop Pattern table); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Measurement-Loop Pattern table
IPP5B	**Burst Refresh IPP Current (1X REF)** Same condition with IDD5B
IDD5F2	**Burst Refresh Current (2X REF)** tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** Same condition with IDD5F2
IDD5F4	**Burst Refresh Current (4X REF)** tRFC=tRFC_x4, Other conditions: see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** Same condition with IDD5F4
IDD6N	**Self Refresh Current: Normal Temperature Range** T_C: 0 to 85°C; LP ASR: Normal*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** Same condition with IDD6N
IDD6E	**Self-Refresh Current: Extended Temperature Range** T_C: 0 to 95°C; LP ASR: Extended*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Extended temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** Same condition with IDD6E
IDD6R	**Self-Refresh Current: Reduced Temperature Range** T_C: 0 to 45°C; LP ASR: Reduced*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Reduced temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** Same condition with IDD6R
IDD6A	**Auto Self Refresh Current** T_C: 0 to 95°C; LP ASR: Auto*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Measurement-Loop Pattern table; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: auto self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6A	**Auto Self Refresh IPP Current** Same condition with IDD6A

IDD7	**Operating Bank Interleave Read Current** CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Measurement-Loop Pattern table; BL: 8*1 ; AL: CL-1; CS_n: H between ACT and RDA; Command, address, bank group address, bank address Inputs: partially toggling according to Measurement-Loop Pattern table; data I/O: read data bursts with different data between one burst and the next one according to Measurement-Loop Pattern table; DM_n: stable at 1; bank activity: two times interleaved cycling through banks (0, 1, …7) with different addressing, see Measurement-Loop Pattern table; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Measurement-Loop Pattern table
IPP7	**Operating Bank Interleave Read IPP Current** Same condition with IDD7
IDD8	**Maximum Power Down Current** TBD
IPP8	**Maximum Power Down IPP Current** Same condition with IDD8

Note:

1. Burst Length: BL8 fixed by MRS: MR0 bits A[1,0] = [0,0].
2. MR: Mode Register
   Output buffer enable:
   set MR1 bit A12 = 0: Qoff = output buffer enabled
   and MR1 bits A[2, 1] = [0,0]: output driver impedance control = RZQ/7
   RTT_Nom enable:
   set MR1 bits A[10:8] = [0,1,1]: RTT_Nom = RZQ/6
   RTT_WR enable:
   set MR2 bits A[11:9] = [0,0,1]: RTT_WR = RZQ/2
   RTT_PARK disable:
   set MR5 bits A[8:6] = [0,0,0]
3. CAL enabled:
   set MR4 bits A[8:6] = [0,0,1]: 1600MT/s;
   [0,1,0]: 1866MT/s, 2133MT/s;
   [0,1,1]: 2400MT/s
   [0,1,1]: 2666MT/s
   [1,0,0]: 3200MT/s
   Gear down mode enabled :
   set MR3 bit A3 = 1: 1/4 Rate
   DLL disabled:
   set MR1 bit A0 = 0
   CA parity enabled:
   set MR5 bits A[2:0] = [0,0,1]: 1600MT/s,1866MT/s, 2133MT/s
   [0,1,0]: 2400MT/s, 2666MT/s
   [0,1,1]: 3200MT/s
   Read DBI enabled:
   set MR5 bit A12 = 1
   Write DBI enabled:
   set :MR5 bit A11 = 1
4. Low Power Array Self-Refresh (LP ASR)
   set MR2 bits A[7:6] = [0,0]: Normal
   [0,1]: Reduced temperature range
   [1,0]: Extended temperature range
   [1,1]: Auto self-refresh

IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Note :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00 D1=FF D2=FF D3=00 D4=FF D5=00 D6=00 D7=FF
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC +nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0=FF D1=00 D2=00 D3=FF D4=00 D6=FF D7=00
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1instead																
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																

		8	7*nRC	repeat Sub-Loop 1, use BG[1:0]^2 = 1, BA[1:0] = 0 instead	
		9	9*nRC	repeat Sub-Loop 1, use BG[1:0]^2 = 2, BA[1:0] = 0instead	For x4 and x8 only
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 1instead	
		11	11*nRC	repeat Sub-Loop 1, use BG[1:0]^2 = 2, BA[1:0] = 2 instead	
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 3instead	
		13	13*nRC	repeat Sub-Loop 1, use BG[1:0]^2 = 2, BA[1:0] = 1instead	
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 2 instead	
		15	15*nRC	repeat Sub-Loop 1, use BG[1:0]^2 = 2, BA[1:0] = 3 instead	
		16	16*nRC	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 0instead	

Note :

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2N_par, IPP2, IDD3N, IDD3NA, and IDD3P Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0]^2 = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, use BG[1:0]^2 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, use BG[1:0]^2 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0]^2 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, use BG[1:0]^2 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0]^2 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, use BG[1:0]^2 = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 0 instead																
		9	36-39	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, use BG[1:0]^2 = 3, BA[1:0] = 0 instead																

Note :

1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			3	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]^2 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]^2 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]^2 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]^2 = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]^2 = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]^2 = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]^2 = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]^2 = 3, BA[1:0] = 0 instead																

Note :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00 D1=FF D2=FF D3=00 D4=FF D5=00 D6=00 D7=FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF D1=00 D2=00 D3=FF D4=00 D5=FF D6=FF D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

Note :

1. QS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command

IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00 D1=FF D2=FF D3=00 D4=FF D5=00 D6=00 D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF D1=00 D2=00 D3=FF D4=00 D5=FF D6=FF D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

Note :

1. DQS_t, DQS_c are used according to W R Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command

IDD4WC Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00 D1=FF D2=FF D3=00 D4=FF D5=00 D6=00 D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF D1=00 D2=00 D3=FF D4=00 D5=FF D6=FF D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	15-19	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	20-24	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	25-29	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	30-34	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	35-39	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	40-44	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	50-54	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	55-59	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	60-64	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	65-69	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	70-74	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	75-79	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

Note :

1. DQS_t, DQS_c are used according to W R Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command

IDD5B Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	REF	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			5-8	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
			9-12	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
			13-16	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
			17-20	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
			21-24	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
			25-28	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
			29-32	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
			33-36	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
			37-40	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
			41-44	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
			45-48	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
			49-52	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
			53-56	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
			57-60	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
			61-64	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 0 instead																
		2	65... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

Note :

1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

IDD7 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	D0=00 D1=FF D2=FF D3=00 D4=FF D5=00 D6=00 D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD +1	RDA	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	D0=FF D1=00 D2=00 D3=FF D4=00 D5=FF D6=FF D7=00
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																

IDD7 Measurement-Loop Pattern[1]- continued

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[13:11]	A[10]/ AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

Note :

1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

Electrical Specifications

IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

IDD and IDDQ Specification

Symbol	DDR4-2400	DDR4-2666	DDR4-3200	Unit
IDD0	113	116	122	mA
IDD0A	113	116	122	mA
IDD1	143	158	188	mA
IDD1A	147	160	186	mA
IDD2N	90	93	99	mA
IDD2NA	90	93	99	mA
IDD2NT	130	135	145	mA
IDD2NL	83	85	89	mA
IDD2NG	85	90	100	mA
IDD2ND	67	70	76	mA
IDD2N_par	102	106	114	mA
IDD2P	60	65	75	mA
IDD2Q	90	95	105	mA
IDD3N	110	115	125	mA
IDD3NA	110	115	125	mA
IDD3P	90	95	105	mA
IDD4R	232	245	271	mA
IDD4RA	242	265	311	mA
IDD4RB	222	235	261	mA
IDD4W	268	290	334	mA
IDD4WA	270	319	417	mA
IDD4WB	251	275	323	mA
IDD4WC	258	280	324	mA
IDD4W_par	260	280	320	mA
IDD5B	195	200	210	mA
IDD5F2	210	220	240	mA
IDD5F4	170	180	200	mA
IDD7	285	345	465	mA
IDD8	35	35	35	mA

IPP Specification

Symbol	DDR4-2400	DDR4-2666	DDR4-3200	Unit
IPP0	8	9	11	mA
IPP1	8	9	11	mA
IPP2N	6	7	9	mA
IPP2P	6	7	9	mA
IPP3N	6	7	9	mA
IPP3P	6	7	9	mA
IPP4R	6	7	9	mA
IPP4W	6	7	9	mA
IPP5B	24	27	33	mA
IPP5F2	25	29	37	mA
IPP5F4	18	20	24	mA
IPP7	33	40	54	mA
IPP8	2	3	5	mA

IDD6 Specification

Symbol	Temperature Range	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		IDD (max)	IPP (Max)	IDD (max)	IPP (Max)	IDD (max)	IPP (Max)		
IDD6N	0 - 85°C	40	6	40	6	40	6	mA	1
IDD6E	0 - 95°C	45	8	45	8	45	8	mA	2
IDD6R	0 - 45°C	35	4	35	4	35	4	mA	3
IDD6A	0 - 85°C	40	6	40	6	40	6	mA	4

Note :

1. Applicable for MR2 settings A6 = 0 and A7 = 0
2. Applicable for MR2 settings A6 = 0 and A7 = 1. IDD6E is only specified for devices which support the extended temperature range feature
3. Applicable for MR2 settings A6 = 1 and A7 = 0. IDD6R is only specified for devices which support the reduced temperature range feature
4. Applicable for MR2 settings A6 = 1 and A7 = 1. IDD6A is only specified for devices which support the auto self-refresh feature

Input/Output Capacitance

Silicon pad I/O Capacitance

Symbol	Parameter	DDR4- 2400/ 2666		DDR4- 3200		Units	Note
		Min.	Min.	Min.	Max.		
CIO	Input/output capacitance	0.55	1.15	0.55	1.00	pF	1,2,3
CDIO	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
CDDQS	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
CCK	Input capacitance, CK_t and CK_c	0.2	0.7	0.2	0.7	pF	1,3
CDCK	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
CI	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.7	0.2	0.55	pF	1,3,6
CDI_ CTRL	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
CDI_ ADD_CMD	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
CALERT	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
CZQ	Input/output capacitance of ZQ	-	2.3	-	2.3	pF	1,3,12
CTEN	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

Note:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_C)
6. CI applies to ODT, CS_n, CKE, A0-A15, BA0-BA1, BG0-BG1, RAS_n, CAS_n/A15, W E_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A15, BA0-BA1, BG0-BG1,RAS_n, CAS_n/A15, W E_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))
12. Maximum external load capacitance on ZQ pin: TBD.
13. TEN pin is DRAM internally pulled low through a weak pull-down resistor to VSS.

DRAM package electrical specifications

Symbol	Parameter	DDR4- 2400/ 2666/ 3200		Units	Note
		Min.	Max.		
Z_{IO}	Input/output Zpkg	45	85	Ω	1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{io}	Input/Output Lpkg	-	3.4	nH	1,2
C_{io}	Input/Output Cpkg	-	0.82	pF	1,3
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85	Ω	1
$Td_{IO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	45	ps	1
$L_{io\ DQS}$	DQS Lpkg	-	3.4	nH	1,2
$C_{io\ DQS}$	DQS Cpkg	-	0.82	pF	1,3
$DZ_{DIO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	Ω	-
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
$Z_{I\ CTRL}$	Input- CTRL pins Zpkg	50	90	Ω	1
$T_{dI_\ CTRL}$	Input- CTRL pins Pkg Delay	14	42	ps	1
$L_{i\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	1,2
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	1,3
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90	Ω	1
$Td_{IADD_\ CMD}$	Input- CMD ADD pins Pkg Delay	14	52	ps	1
$L_{i\ ADD\ CMD}$	Input CMD ADD Lpkg	-	3.9	nH	1,2
$C_{i\ ADD\ CMD}$	Input CMD ADD Cpkg	-	0.86	pF	1,3
Z_{CK}	CLK_t & CLK_c Zpkg	50	90	Ω	1
Td_{CK}	CLK_t & CLK_c Pkg Delay	14	42	ps	1
$L_{i\ CLK}$	Input CLK Lpkg	-	3.4	nH	1,2
$C_{i\ CLK}$	Input CLK Cpkg	-	0.7	pF	1,3
DZ_{DCK}	Delta Zpkg CLK_t & CLK_c	-	10	Ω	-
D_{TdCK}	Delta Delay CLK_t & CLK_c	-	5	ps	-
Z_{OZQ}	ZQ Zpkg	-	100	Ω	-
$Td_{O\ ZQ}$	ZQ Delay	20	90	ps	-
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	Ω	-
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	-

Note:
1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

Standard Speed Bins

DDR4-2400 Speed Bins

Speed Bins				DDR4-2400 (17-17-17)		Unit	Note
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.16[12] (13.75)[5,10]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	10
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5,10]	-	ns	10
PRE command period			tRP	14.16 (13.75)[5,10]	-	ns	10
ACT to PRE command period			tRAS	32	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	46.16 (45.75)[5,10]	-	ns	10
	Normal	**Read DBI**					
CWL =9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
				(Optional)[5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,6
				(Optional)[5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,6
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4,6
				(Optional)[5,10]			
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3,6
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.938	ns	
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.938	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	11
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

DDR4-2666 Speed Bins

Speed Bins				DDR4-2666 (19-19-19)		Unit	Note
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.25[12] (13.75)[5,10]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	10
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5,10]	-	ns	10
PRE command period			tRP	14.25 (13.75)[5,10]	-	ns	10
ACT to PRE command period			tRAS	32	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	46.25 (45.75)[5,10]	-	ns	10
	Normal	**Read DBI**					
CWL =9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
				(Optional)[5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
				(Optional)[5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,7
				(Optional)[5,10]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,7
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,7
				(Optional)[5,10]			
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20		nCK	11
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

DDR4-3200 Speed Bins

Speed Bins				DDR4-3200 (24-24-24)		Unit	Note
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	15.00	19.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(min) + 4nCK	ns	10
ACT to internal read or write delay time			tRCD	15.00	-	ns	10
PRE command period			tRP	15.00	-	ns	10
ACT to PRE command period			tRAS	32	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	tRAS + tRP	-	ns	10
	Normal	**Read DBI**					
CWL =9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.9	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,8
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 19	CL = 22	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,8
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.682	ns	1,2,3
Supported CL Settings				10,12,14,16,18,20,22,24		nCK	11
Supported CL Settings with read DBI				12,14,16,19,21,23,28		nCK	
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	

Speed Bin Table Notes

Absolute Specification

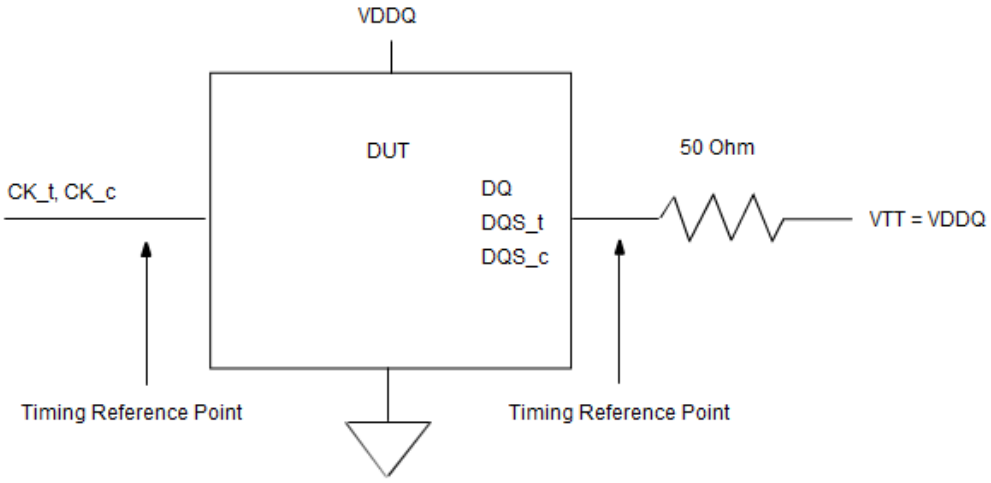
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-2400, 2666 and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938, 0.833, 0.750 or 0.625 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns, 0.833 ns, 0.750 ns or 0.625 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
10. Parameter apply from tCK(avg)min to tCH(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
11. CL number in parentheses, it means that these numbers are optional.
12. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

Electrical Characteristics & AC Timing

Reference Load for AC Timing and Output Slew Rate

Figure represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.
It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Reference Load for AC Timing and Output SlewRate

tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

tREFI by device density

Parameter	Symbol		4Gb	Units
Average periodic refresh interval	tREFI	$0°C \leqq T_C \leqq 85°C$	7.8	us
		$85°C < T_C \leqq 95°C$	3.9	us

Timing Parameters by Speed Grade

Timing Parameters by Speed Bin for DDR4-2400

Parameter	Symbol	DDR4-2400		Units	Note
		Min.	Max.		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns	
Average Clock Period	tCK(avg)	0.833	< 0.938	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min _ tot	tCK(avg)max + tJIT(per)max _ tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-42	42	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	83		ps	25
Cycle to Cycle Period Jitterdeterministic	tJIT(cc)_dj	42		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	67		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-112	112	ps	
Cumulative error across 13 cycles	tERR(13per)	-114	114	ps	
Cumulative error across 14 cycles	tERR(14per)	-116	116	ps	
Cumulative error across 15 cycles	tERR(15per)	-118	118	ps	
Cumulative error across 16 cycles	tERR(16per)	-120	120	ps	
Cumulative error across 17 cycles	tERR(17per)	-122	122	ps	
Cumulative error across 18 cycles	tERR(18per)	-124	124	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps	

Timing Parameters by Speed Bin for DDR4-2400- continued

Parameter	Symbol	DDR4-2400		Units	Note
		Min.	Max.		
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) /Vil(ac) levels	tIS(base)	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	162	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	162	-	ps	
Control and Address Input pulse width for each input	tIPW	410	-	ps	
Command and AddressTiming					
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5.000ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (1K)	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/ 2K)	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	-		1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-		

Timing Parameters by Speed Bin for DDR4-2400- continued

Parameter	Symbol	DDR4-2400		Units	Note
		Min.	Max.		
WRITE recovery time	tWR	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tW R+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC _DM	tW TR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC _DM	tW TR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	nCK	
Mode Register Set command update delay	tMOD	Max (24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	33
Multi Purpose Register W rite Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK	
CS_n to Command Address Latency					
CS_n to Command Address Latency	tCAL	5	-	nCK	
DRAM Data Timing					
DQS_t,DQS_c to DQ skew,per group, per access	tDQSQ	-	TBD	tCK(avg) /2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	tCK(avg) /2	13,17, 18
DQS_t, DQS_c differential READ Preamble(1 clock preamble)	tRPRE	0.9	TBD	tCK	
DQS_t, DQS_c differential READ Preamble(2 clock preamble)	tRPRE	1.8	TBD	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	tCK	
DQS_t, DQS_c differential output high time	tQSH	0.4	-	tCK	21
DQS_t, DQS_c differential outputlow time	tQSL	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-300	150	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	150	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK	

Timing Parameters by Speed Bin for DDR4-2400- continued

Parameter	Symbol	DDR4-2400		Units	Note
		Min.	Max.		
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK	-175	175	ps	
MPSM Timing					
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-		
Calibration Timing					
Power-up and RESET calibration time	tZQinit	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	nCK	
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC (min) + 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-		
SRX to commands not requiring a locked DLL in Self RefreshABORT	tXS_ABORT (min)	tRFC4(min) + 10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min) + 10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1 nCK	-		

Timing Parameters by Speed Bin for DDR4-2400- continued

Parameter	Symbol	DDR4-2400		Units	Note
		Min.	Max.		
Minimum CKE low width for Self re- fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min) + 1nCK + PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns) + PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-		
Power Down Timing					
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	Max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tW R/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP - BC4DEN	WL+2+(tW R/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP - BC4DEN	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-		
PDA Timing					
Mode Register Set command cycle time in PDA mode	tMRD_PDA	Max	(16nCK, 10ns)		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD			

Timing Parameters by Speed Bin for DDR4-2400- continued

Parameter	Symbol	DDR4-2400		Units	Note
		Min.	Max.		
ODT Timing					
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	
Write Leveling Timing					
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	12
DQS_t/DQS_n delay after write level- ing mode is programmed	tWLDQSEN	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	ns	
Write leveling output error	tWLOE			ns	
CA Parity Timing					
Commands not guaranteed to be ex- ecuted during this time	tPAR_UN-KNOWN	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	64	nCK	
Parity Latency	PL	5		nCK	
CRC Error Reporting					
CRC error to ALERT_nlatency	tCRC_ALERT	3	13	ns	
CRC ALERT_n pulsewidth	CRC_ALERT_PW	6	10	nCK	
tREFI					
tRFC1 (min)	4Gb	260	-	ns	34
tRFC2 (min)	4Gb	160	-	ns	34
tRFC4 (min)	4Gb	110	-	ns	34

Timing Parameters by Speed Bin for DDR4-2666/3200

Parameter	Symbol	DDR4-2666		DDR4-3200		Units	Note
		Min.	Max.	Min.	Max.		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	ns	
Average Clock Period	tCK(avg)	0.750	<0.833	0.625	<0.682	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min _ tot	tCK(avg)max + tJIT(per)max _ tot	tCK(avg)min + tJIT(per)min _ tot	tCK(avg)max + tJIT(per)max _ tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-38	38	-32	32	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-30	30	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	75		-	62	ps	
Cycle to Cycle Period Jitterdeterministic	tJIT(cc)_dj	38		32		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	60		-	62	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-55	55	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-66	66	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-73	73	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-78	78	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-83	83	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-87	87	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-91	91	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-94	94	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-96	96	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-99	99	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-101	101	-84	84	ps	
Cumulative error across 13 cycles	tERR(13per)	-103	103	-86	86	ps	
Cumulative error across 14 cycles	tERR(14per)	-104	104	-87	87	ps	
Cumulative error across 15 cycles	tERR(15per)	-106	106	-89	89	ps	
Cumulative error across 16 cycles	tERR(16per)	-108	108	-90	90	ps	
Cumulative error across 17 cycles	tERR(17per)	-110	110	-92	92	ps	
Cumulative error across 18 cycles	tERR(18per)	-112	112	-93	93	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	

Timing Parameters by Speed Bin for DDR4-2666/3200- continued

Parameter	Symbol	DDR4-2666		DDR4-3200		Units	Note
		Min.	Max.	Min.	Max.		
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) /Vil(ac) levels	tIS(base)	55	-	40	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	145	-	130	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	80	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	145	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	385	-	340	-	ps	
Command and AddressTiming							
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5ns)	-	Max(4nCK, 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (1K)	Max(4nCK, 3ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/ 2K)	Max(4nCK, 3ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 12ns)	-	Max(16nCK, 10ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	nCK	1,2,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	nCK	1,34
Internal READ Command to PRECHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	nCK	34

Timing Parameters by Speed Bin for DDR4-2666/3200- continued

Parameter	Symbol	DDR4-2666		DDR4-3200		Units	Note
		Min.	Max.	Min.	Max.		
WRITE recovery time	tWR	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK, 3.75ns	-	tWR+max (5nCK, 3.75ns	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max (5nCK, 3.75ns)	-	tWTR_S+max (5nCK, 3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (5nCK, 3.75ns)	-	tWTR_L+max (5nCK, 3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	854	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)		max(24nCK, 15ns)		nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	33
Multi Purpose Register W rite Recovery Time	tWR_MPR	MIN = tMOD + AL + PL; MAX = N/A				-	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		MIN = WR + ROUNDtRP/tCK (AVG); MAX = N/A		nCK	
CS_n to Command Address Latency							
CS_n to Command Address Latency	tCAL	5	-	6	-	nCK	
DRAM Data Timing							
DQS_t,DQS_c to DQ skew,per group, per access	tDQSQ	-	0.18	-	0.20	tCK(avg) /2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	0.74	-	0.70	-	tCK(avg) /2	13,17, 18
DQS_t, DQS_c differential READ Preamble(1 clock preamble)	tRPRE	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential READ Preamble(2 clock preamble)	tRPRE	1.8	-	1.8	-	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	0.33	-	tCK	
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	tCK	21
DQS_t, DQS_c differential outputlow time	tQSL	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-310	170	-250	160	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	-	160	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	tCK	

Timing Parameters by Speed Bin for DDR4-2666/3200- continued

Parameter	Symbol	DDR4-2666		DDR4-3200		Units	Note
		Min.	Max.	Min.	Max.		
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK	-170	170	-160	160	ps	
MPSM Timing							
Command path disable delay upon MPSM entry	tMPED	MIN = tMOD (MIN) + tCPDED (MIN) ; MAX = N/A				nCK	
Valid clock requirement after MPSM entry	tCKMPE	MIN = tMOD (MIN) + tCPDED (MIN) ; MAX = N/A				nCK	
Valid clock requirement before MPSM exit	tCKMPX	MIN = tCKSRX (MIN) ; MAX = N/A				nCK	
Exit MPSM to commands not requiring a locked DLL	tXMP	MIN = tXS (MIN) ; MAX = N/A				nCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	MIN = tXMP (MIN) + tXSDLL (MIN) ; MAX = N/A				nCK	
CS setup time to CKE	tMPX_S	MIN = tIS (MIN) + tIH (MIN) ; MAX = N/A				ns	
CS_n High hold time to CKE	tMPX_HH	tXP	-	tXP	-	ns	
CS_n Low hold time to CKE	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	ns	
Calibration Timing							
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	nCK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK, tRFC(min)+ 10ns)	-	max (5nCK, tRFC(min)+ 10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self RefreshABORT	tXS_ABORT (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to commands re-quiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+ 1 nCK	-	tCKE(min)+ 1 nCK	-	nCK	

Timing Parameters by Speed Bin for DDR4-2666/3200- continued

Parameter	Symbol	DDR4-2666		DDR4-3200		Units	Note
		Min.	Max.	Min.	Max.		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK,5ns)	-	max (3nCK,5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG) ; MAX = N/A				nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	MIN = WL + 4 + WR + 1 ; MAX = N/A				nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP - BC4DEN	MIN = WL + 2 + tWR/tCK (AVG) ; MAX = N/A				nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP - BC4DEN	MIN = WL + 2 + WR + 1 ; MAX = N/A				nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (MIN)	-	tMOD (MIN)	-	nCK	
PDA Timing							
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max (16nCK,10ns)	-	max (16nCK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD	-	tMOD	-	nCK	

Timing Parameters by Speed Bin for DDR4-2666/3200- continued

Parameter	Symbol	DDR4-2666		DDR4-3200		Units	Note
		Min.	Max.	Min.	Max.		
ODT Timing							
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.26	0.74	tCK(avg)	
Write Leveling Timing							
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write level- ing mode is programmed	tWLDQSEN	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ ALERT_ON	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ ALERT_PW	80	160	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ ALERT_RSP	-	71	-	85	nCK	
Parity Latency	PL	5		6	-	nCK	
CRC Error Reporting							
CRC error to ALERT_nlatency	tCRC_ALERT	3	13	3	13	ns	
CRC ALERT_n pulsewidth	CRC_ ALERT_PW	6	10	6	10	nCK	
Geardown setup time	tGEAR_setup	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	2	-	2	-	nCK	
tREFI							
tRFC1 (min)	4Gb	260	-	260	-	ns	34
tRFC2 (min)	4Gb	160	-	160	-	ns	34
tRFC4 (min)	4Gb	110	-	110	-	ns	34

Note:

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after W L.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after W L.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tW RPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on T_C.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled, tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled, tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks.
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg) min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg) min/2.

Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

Function Matrix (By ORG. V:Supported, Blank:Not supported)

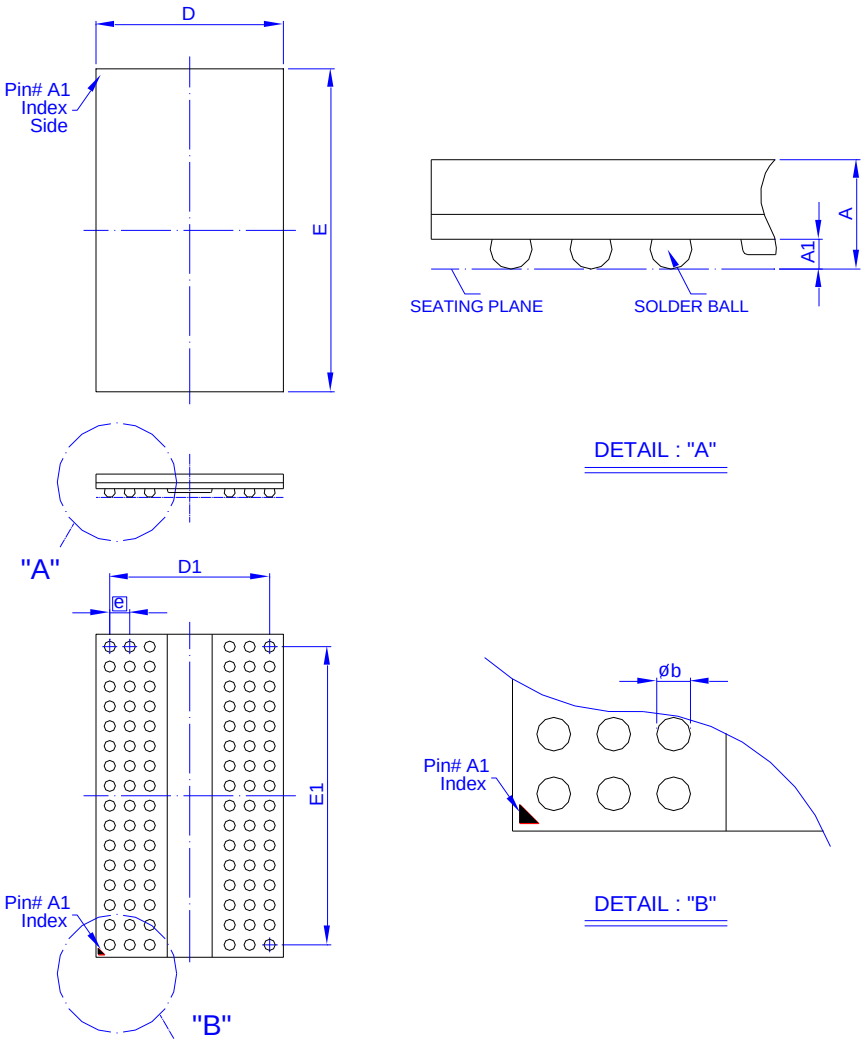
Functions	x4	x8	x16	Note
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask		V	V	
Data Bus Inversion		V	V	
TDQS		V		
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V	V	
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode	V	V	V	
Programmable Preamble	V	V	V	
Maximum Power Down Mode	V	V		
Boundary Scan Mode			V	
Additive Latency	V	V		

Function Matrix (By Speed. V:Supported, Blank:Not supported)

Functions	DLL Off mode	DLL On mode			Note
	equal or slower	2133 Mbps	2400 Mbps	2666/3200 Mbps	
Write Leveling	V	V	V	V	
Temperature controlled Refresh	V	V	V	V	
Low Power Auto Self Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi Purpose Register	V	V	V	V	
Data Mask	V	V	V	V	
Data Bus Inversion	V	V	V	V	
TDQS		V	V	V	
ZQ calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Readout	V	V	V	V	
CAL		V	V	V	
WRITE CRC		V	V	V	
CA Parity		V	V	V	
Control Gear Down Mode				V	
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Down Mode		V	V	V	
Boundary Scan Mode	V	V	V	V	

PACKING DIMENSIONS

96-BALL DDR SDRAM (7.5x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.00	—	—	0.039
A_1	0.30	0.35	0.40	0.012	0.014	0.016
Φ_b	0.40	0.45	0.50	0.016	0.018	0.020
D	7.40	7.50	7.60	0.291	0.295	0.299
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1	6.40 BSC			0.252 BSC		
E_1	12.00 BSC			0.472 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter.

(Revision date : Nov172 2017)

Revision History

Revision	Date	Description
0.1	2019.08.21	Original
1.0	2019.11.19	Delete Preliminary
1.1	2020.01.03	1. Add speed grade 2600Mbps and 3200Mbps 2. Correct typo
1.2	2020.08.28	1. Modify the description of feature 2. Modify IDD and IDDQ Specification
1.3	2022.06.02	Add Functional Description
1.4	2022.10.17	Correct Output Driver Impedance Control table

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